A Transformer Feedback CMOS LNA for UWB Application

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Abstract—A transformer feedback low-noise amplifier (LNA) is implemented in a standard 0.18 μm CMOS process, which exploits drain-to-gate transformer feedback technique for wideband input matching and operates across entire 3–5 GHz ultra-wideband (UWB). The proposed LNA achieves power gain above 9.5 dB, input return loss less than 15.0 dB, and noise figure below 4.8 dB, while consuming 8.1 mW from a 1.8-V supply. To the authors’ knowledge, drain-to-gate transformer feedback for wideband input matching cascode LNA is the first adopted technique for UWB application.

Index Terms—Transformer feedback, wideband input matching, LNA, CMOS, UWB

I. INTRODUCTION

Despite of the slight difference in worldwide, ultra-wideband (UWB) system using the unlicensed frequency band from 3.1 to 10.6 GHz has been drawing attention as a technical solution for the low power and high data-rate wireless communications systems. Especially, 3–5 GHz frequency bands are used for indoor communication and sensor application in Japan, Europe, and Korea.

One of the most critical blocks in the UWB receiver is the low-noise and wideband amplifier since LNA have a great impact on receiver performance such as the sensitivity. Especially, LNA should provide a low noise figure and gain flatness through the entire UWB frequency band while maintaining wideband input matching. Various UWB LNA topologies for wideband input matching have been reported such as the LC ladder [1], common-gate (CG) amplifier, and resistive shunt feedback [2]. The LC ladder topology incorporating on-chip inductor and capacitor as a matching network shows good performance for wideband matching. However, the adoption of the LC filter at the input stage mandates a number of reactive components, which occupies large chip area and deteriorates noise performance. CG amplifier also has wideband input characteristic due to its intrinsic low input impedance (~1/gm), but usually has poor noise performances and trade-off between the gain and input matching. Another approach for wideband input matching is the resistive shunt feedback LNA, which accompanies with degradation of the noise performance due to feedback resistor and trade-offs between NF and input matching.

Among the various wideband input matching topologies, a reactive (transformer) feedback is one of the applicable candidates in respect of the area efficiency and the moderate NF degradation. Up to now, numerous transformer feedback structures have been published [3-7]. Reactive components should be used inevitably for wideband input and output matching or inter-stage matching [1], while the silicon area increases in comparison with resistive feedback or CG amplifier. Therefore, the feedback topology using reactive component such as an integrated transformer is useful technique to design the wideband LNA. The reactive feedback LNA using integrated transformers also has the virtue of providing DC coupled bias and lower noise.
contribution. Therefore, the integrated transformer is greatly attractive component due to its area efficiency while providing two or more reactance.

This paper is organized as follows. In section II, the proposed Drain-Gate (D-G) reactive feedback topology is introduced at first. In section III, circuit description is presented in detail with the analytical expressions of its input impedance and voltage gain. The experimental results along with the comparison to prior arts are presented in section IV. Finally, the conclusions are followed in section V.

II. PROPOSED D-G REACTIVE FEEDBACK TOPOLOGY

In previously published literature [3], reactive D-G feedback topology is adopted to neutralize the gate-drain capacitance (Cgd) by Miller multiplication; as a result the stability of amplifier is improved over a wide bandwidth. However, Miller effect is less significant in cascode structure due to unity voltage gain [5]. Infeed from drain to gate in cascode LNA can be applicable as an alternative way to achieve transformer feedback from drain to gate in cascode LNA part. Since for low values which for high voltage gain and input 50-Ω matching with respect to the turn-ratio [8].

To overcome this limitation, the cascode structure has been adopted, and the lower input admittance (~20 mS) can be achieved while gdo is high enough to have proper voltage gain of the LNA through selecting the turn-ratio carefully (e.g., gdo is 40 mS~50 mS, k/n is 0.5).

III. CIRCUIT DESCRIPTION

1. D-G Feedback LNA

The schematic of the proposed UWB LNA consists of two stage amplifier, including source follower buffer for measurement purpose, as shown in Fig. 2. The main stage is the common-source (CS) amplifier with reactive feedback using on-chip transformer. As a cascode structure, CG transistor (M2) was inserted to obtain a high gain and good reverse isolation at the same time.

![Fig. 1. Transformer based drain-gate feedback topology.](image)

\( Y_\text{in}(s) = \frac{g_m}{n^2} + \frac{g_m}{n} \frac{k}{n} + \frac{1}{sL_2} + sC_g \)  

\( \frac{V_o}{V_\text{in}}(s) = -\frac{g_m \cdot sL_2 + (k/n)}{1 + sL_2 \cdot g_m}, L_2 = L_2 \cdot (1-k^2) \)  

where \( g_m \) is the device transconductance, \( g_o \) is the output conductance, and \( C_g \) is the input capacitance of the LNA. Also, the transformer coefficients can be design parameters such as coupling factor (k), turn ratio \( n^2 = L_2/L_1 \), and mutual inductance \( M = k \sqrt{L_1 L_2} \) of the transformer. In Eq. (1), if the second term of denominator is carefully selected to be less than one, the real term of \( Y_\text{in}(s) \) can be expressed as follows,

\[ \text{Re}\{Y_\text{in}(s)\} = g_m \frac{k}{n} \]  

Since the input impedance is a function of transformer parameters, applying reactive feedback to match the amplifier input stage with 50-Ω is feasible. One drawback of this topology is that the trade-off exists between a high voltage gain and input 50-Ω matching.
For the DC blocking purpose, $C_b$ and $C_c$ are added at the input/output of LNA. Although feedforward effects are minor due to relatively lower current at the input stage in comparison to the output, the feedback resistor $R_o$, which is located between the input and the self-inductance $L_1$, acts as a feedforward controller by adjusting a signal current at the feedback path of LNA.

Knowing from Eqs. (1, 3), 20-mS input admittance can be achieved in the range of the resonant frequency ($1/\sqrt{L_1C_g}$). For the low-band UWB (3–5 GHz) input matching, the series inductor $L_g$ is added to cancel out the imaginary part. Without $L_g$ for simplification, the calculated input impedance of LNA can be described as Eq. (4) including the effects of the feedback and $R_c$.

$$Z_{in}(s) = \frac{sL_1 + R_f}{1 + (g_{m1} + sC_g) \cdot (R_d + sL_2)} \quad / / sC_g \quad (4)$$

$$\frac{V_{dL}}{V_{st}}(s) = \frac{-g_{m1} \cdot sL_2 + R_d}{1 + sL_1 + (g_{m1} + sC_g) \cdot sL_1} \cdot \frac{k}{n}$$

$$\quad + \frac{R_f}{sL_1} \cdot (R_d + sL_2) + \frac{k}{n} \quad (5)$$

Eq. (5) is also depicted as a transfer function taking the feedforward effects into consideration. The first step in this design, the input transistor is carefully sized as a compromise between gain ($g_{m1}$ with a current bias) and input impedance matching. Once the transistor aspect ratio ($W/L$) has been selected, the device transconductance is fixed for a given choice of bias current (in this case 4.5 mA). From Eq. (4), the second term in numerator determines a real term of the input impedance. Also, in order to obtain a broadband response, the shunt peaking load is employed using a resistor $R_d$ and self-inductance $L_2$, which is a part of on-chip transformer. The effective bandwidth can be extended by optimizing the self-inductance $L_2$. After carefully choosing the transconductance of input transistor and the self-inductance $L_2$, the turn-ratio of the transformer attaining the input matching to 50-Ω is determined from the feedback factor ($k/n$) in Eq. (4).

The simulated input matching $S_{11}$ with a series inductor $L_g$ is shown in Fig. 3(a). To achieve the input matching of the entire low-band UWB, a complex zero is placed around 4.0 GHz through the considerate selection of the design variables, such as transformer parameters and $L_g$. By optimizing the feedback factor ($k/n$) and $g_{m1}$, the calculated real-term of the input impedance can be close to 50-Ω from 2.5 GHz to 6.8 GHz as shown in Fig. 3(b). Thus, the proposed D-G reactive feedback paves the way for broadband input matching using on-chip transformer.

2. Transformer Design for Reactive Feedback

In the design of the wideband transformer feedback LNA, the parameters of active transistor and parasitic components in the transformer determine the input reflection coefficient. Also, the circuit layout plays a critical role in the design of wideband circuit.

Thus, the layout of transformer should be co-designed with that of active transistors for both miniaturizing the geometry and minimizing the effects of layout parasitic. The layout of the D-G Transformer is shown in Fig. 4. Especially, since the self-inductance ($L_2$) acts as a shunt peaking load to obtain a broadband response, the
significant transformer parameters such as self-inductance, turn ratio, and coupling factor should be accurately extracted and modeled through the reliable electro-magnetic (EM) tools to achieve the desired performance.

Ultimately, the transformer geometry and parameters are optimized to obtain the wideband 50-Ω input matching. From the iterative EM simulation and optimization, the inner diameters of self-inductor L₁ and L₂ are designed to be 20 μm and 30 μm, respectively, which lead to the total area of 330 x 330 μm². Also, the metal width and spacing are 4 μm and 6 μm to have the wanted inductances and Q-factor, respectively. EM simulation reveals that the optimized values of self-inductances are L₁ = 3.9 nH and L₂ = 4.8 nH at 4.0 GHz, and the obtained mutual inductance is 1.76 nH with the coupling factor of 0.72. And both of the self-inductors have same Q-factor of 6 at 4.0 GHz as shown in Fig. 5, respectively. Therefore, the real term of the proposed transformer feedback LNA is using the feedback factor (k/n = 0.8).

### IV. Measurement Results

The proposed D-G transformer feedback LNA is implemented in a 0.18-μm CMOS technology. Fig. 6 shows the chip microphotograph and chip core area without pads is 850 x 350 μm². S-parameters of the proposed D-G transformer feedback LNA were measured by utilizing RF on-chip probing with Agilent E8363C two-port network analyzer. As shown in Fig. 7, the measured input reflection coefficient is below -10 dB from 2.5 GHz to 6.8 GHz and the power gain is more than 9.5 dB in the lower UWB band. The 3-dB bandwidth up to 5.5 GHz can cover the entire lower UWB band. Also, the measured noise figure as shown in Fig. 8 is less than 4.8 dB in the target UWB band. The measured input referred IP3 is higher than -13.0 dBm and the 1-dB compression power is -20.0 dBm in the frequency range of 3~5 GHz. DC measurement reveals the power consumption of 8.1 mW excluding source-follower buffer from a 1.8-V power supply. Circuit performances of the proposed D-G transformer feedback...
LNA and the performance comparison of the previously designed 3-5 GHz UWB LNA are summarized in Table 1.

V. CONCLUSIONS

The proposed D-G transformer feedback LNA has been realized in a 0.18-μm CMOS process. To achieve a wideband input matching, a reactive feedback from drain to gate in the cascade LNA is adopted using on-chip transformer. Also, on-chip transformer and its layout are judiciously designed to obtain the wide-band input matching and the proper gain of LNA, simultaneously. The proposed D-G transformer feedback LNA achieves the power gain more than 9.5 dB and noise figure less than 4.8 dB, while maintaining input impedance matching from 2.5 to 6.8 GHz.

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REFERENCES

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