A 12 bit 750 kS/s 0.13 mW Dual-sampling SAR ADC

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Abstract—A 12-bit 750 kS/s Dual-Sampling Successive Approximation Register Analog-to-Digital Converter (SAR ADC) technique with reduced Capacitive DAC (CDAC) is presented in this paper. By adopting the Adaptive Power Control (APC) technique for the two-stage latched type comparator and using bootstrap switch, power consumption can be reduced and overall system efficiency can be optimized. Bootstrapped switches also are used to enhance the sampling linearity at a high input frequency. The proposed SAR ADC reduces the average switching energy compared with conventional SAR ADC by adopting reduced the Most Significant Bit (MSB) cycling step with Dual-Sampling of the analog signal. This technique holds the signal at both comparator input asymmetrically in sample mode. Therefore, the MSB can be calculated without consuming any switching energy. The prototype SAR ADC was implemented in 0.18-µm CMOS technology and occupies 0.728 mm². The measurement results show the proposed ADC achieves an Effective Number of Bits (ENOB) of 10.73 at a sampling frequency of 750 kS/s and clock frequency of 25 MHz. It consumes only 0.13 mW from a 5.0-V supply and achieves the INL and DNL of +2.78/-2.45 LSB and +0.36/-0.73 LSB respectively, SINAD of 66.35 dB, and a Figures-of-Merit (FoM) of a 102 fJ/conversion-step.

Index Terms—SAR ADC, Bootstrapped switch, CDAC, comparator, dual-sampling, energy-efficient

I. INTRODUCTION

Nowadays, consuming low power is one of the most pressing design concerns for energy-limited applications, such as wireless portable devices and mobile applications. Since Analog-to-Digital Converters (ADCs) are the key blocks of these systems, it is essential to improve the energy efficiency of the ADC to extend the system’s life-span. Among the many types of ADCs, Slope ADC, Sigma-Delta ADC, and Successive Approximation Register (SAR) ADCs are good candidates for low power applications. Especially, the SAR ADC has found wide application for its reasonable resolution, speed, simple structure, and high energy efficiency [1-6].

SAR ADCs are frequently the architecture of choice for medium-to-high-resolution applications with sample rates under 10 mega samples per second (Msps). Resolution for SAR ADCs most commonly ranges from 8 to 16 bits, and they provide low power consumption as well as a small form factor. This combination of features makes these ADCs ideal for a wide variety of applications, such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition.

As the name implies, the SAR ADC basically implements a binary search algorithm. Therefore, while the internal circuitry might be running at several megahertz (MHz), the ADC sample rate is a fraction of that due to the successive-approximation algorithm [5, 6].

This paper describes how the SAR ADC operates by using a binary search algorithm so that the CDAC output converges on the input signal. It also explains the central aspect of the SAR ADC, the capacitive DAC, as well as the high-speed comparator. The paper also describes the reference voltage generator, the relaxation oscillator, new Bandgap Reference (BGR) voltage and the input buffer
This paper presents a power-efficient SAR ADC that combines several techniques to achieve low power design and speed requirements. First, the dual-sampling method is used to reduce the switching energy, reduce the total capacitance, and decrease the layout area and power consumption. Second, bootstrapped switches are used to enhance the sampling linearity at a high input frequency. Finally, the dynamic comparator is adopted to ensure that the power consumption of the comparator scale is proportional to the comparison rate.

The remainder of this paper is organized as follows: Section II describes the proposed ADC architecture. Section III explains the circuit details, including the CDAC, comparator, reference voltage generator, bootstrapped-switch, relaxation oscillator, and input buffer. Section IV then shows the measurement results and section V gives the conclusion.

II. SAR ADC ARCHITECTURE

In the conventional SAR ADC, the capacitance of CDAC is changed and compared to the sampling value, using a binary searching mechanism to define the output code from the MSB to the Least Significant Bit (LSB). The capacitor for CDAC should have $2^n C$ capacitance to satisfy the output resolution. This means that size becomes extremely large when designing high resolution ADCs and the power consumption of the reference generator used as the charging and discharging capacitor increases as a result [3].

Since the proposed dual-sampling SAR ADC structure can be compared to the MSB signal through a sampling process, CDAC can be designed to have $2^{n-1} C$ capacitance. This means that the MSB capacitor can be reduced and consequently, the size and power consumption can be reduced. Moreover, by adopting the APC technique for the comparator, power consumption can be reduced and overall circuit efficiency and performance can be optimized.

Fig. 1(a) shows a diagram of the proposed dual-sampling SAR ADC architecture, while the CDAC structure and its signal timing diagram are shown in Fig. 1(b) and (c), respectively. The ADC architecture consists of a simple analog block, including a binary-weighted CDAC, a comparator, SAR control logic, bootstrapped switches, an input buffer, a reference voltage generator and a RC-oscillator. In this case, the total capacitance is $2^{n-1} C + C_{S&H}$, where $2^{n-1} C$ is the capacitance of CDAC and $C_{S&H}$ is the capacitance of the bootstrapping...
capacitor (Sample & Hold circuit). The analog input voltage \(V_{IN}\) is held on a Sample & Hold. To implement the binary search algorithm, the N-bit register is first set to midscale (that is, 100...00, where the MSB is set to 1).

This forces the DAC output \(V_{DAC}\) to be \(V_{REF}/2\), where \(V_{REF}\) is the reference voltage given to the ADC. A comparison is then performed to determine if \(V_{IN}\) is less than or greater than \(V_{DAC}\). If \(V_{IN}\) is greater than \(V_{DAC}\), the comparator output is a logic high, or 1, and the MSB of the N-bit register remains at 1. Conversely, if \(V_{IN}\) is less than \(V_{DAC}\), the comparator output is a logic low and the MSB of the register is cleared to logic 0. The SAR control logic then moves to the next bit down, forces that bit to be high, and performs another comparison.

The sequence continues down to the LSB. Once this has finished, the conversion is complete and the N-bit digital word is available in the register. In the proposed SAR ADC architecture, analog signals are sampled and held asymmetrically at each input side of the comparator; thus, it is called the dual-sampling method. This operation enabled the MSB to be calculated without consuming any switching energy. In the SAR algorithm, the operation is composed of a sample mode, hold mode, and redistribution mode. The CDAC shown in Fig. 1(b) samples the analog input value in the sample stage. In the hold stage, one side of all capacitors is connected to \(V_{REF}\) and all capacitors hold analog input. In addition, the successive approximation process starts in the redistribution stage. One bit is determined at each cycle and n-cycles are needed for the n-bit digital code conversion [3-5].

Fig. 1(c) shows the timing diagram of the proposed SAR ADC. When the Start of Conversion (SOC) signal is applied, sampling and data conversion begins. Conversely, when the SOC is finished, the End of Conversion (EOC) signal is generated while outputting digital data. In the sample stage, the analog input voltage is sampled during 5 clock cycles. In the hold or comparison stage, the conversion is completed after 12 steps or 32 clock cycles and 2 clock cycles are needed for the end of conversion (EOC) and digital output is obtained. The redundancy SAR algorithm is adopted to correct the error that occurred in each conversion step.

As can be seen in Fig. 1(c), the duration of each conversion step is designed to be variable, considering the settling time of the reference voltage due to the capacitance in DAC. In Step 1 of the comparison stage, the MSB is determined and the reference voltage generator drives the largest capacitance in the DAC. Thus, 5 clock cycles are required to ensure the reference voltage settles and to obtain an MSB bit in Step 1 - 2. Moreover, 34 clock cycles are required for Steps 2 - 12, EOC, and Data Out.

III. ADC CIRCUIT IMPLEMENTATION

1. Dual-sampling SAR ADC Switching Sequence

Fig. 2 indicates the 4-bit switching sequence of the dual-sampling algorithm and the SAR architecture operation. The total capacitance is \(9C_0\). In the SAR architecture described earlier, analog signals are sampled and kept asymmetrically at each input side of the comparator; thus, it is called the dual-sampling method. Using this method, one input side of the comparator is linked to the CDAC and its capacitance is \(\delta C_0\). The other input side of the comparator is linked to \(C_{S&H}\) and its capacitance is \(C\). To save energy during the MSB calculation in the sample mode, the CDAC samples \([V_{ref} - V_{IN}]\), and \(C_{S&H}\) samples \(V_{IN}\) and in hold mode, the MSB are determined differentially by the comparator. From the second cycle, the successive approximation process is conducted differentially.

The state of the comparator input that shows the voltage of CDAC and \(C_{S&H}\) at each cycle is presented in Fig. 2. At the first cycle, bootstrapping by \(C_{S&H}\) is cleared by the MSB. The CDAC operation is independent of the MSB value [3].

2. Comparator

In a 12-bit SAR ADC, the comparator is crucial because its noise performance dominates the ADC resolution. Fig. 3 shows a schematic of the rail-to-rail comparator used in the ADC which consists of a two preamplifier and a dynamic latch structure to achieve fast-decision and high-resolution [7]. The use of a preamplifier at the input stage can reduce the effect of kickback noise. In addition, an adaptive power control technique was applied in this comparator to minimize the current consumption. The APC signal turns off the comparator after the outputs of the comparator are
determined. This APC signal reduces the active time of the comparator, resulting in the reduction of the total power consumption. The APC operation generates a short pulse by gating the ADC clock and the delayed clock. Since the comparison is finished only if the APC signal is high, the APC operates so as to minimize the dynamic current.

N1-N4 and P1-P4 form the phase of the preamplifier, while the output latch stage is formed by P5, P6 and N7, N8. Notably, the NMOS and PMOS merge beside N1, N2 and P1, P2. A rail-to-rail input range is therefore specified for the comparator. In the process of resetting, i.e. when the clock is low, NS1, NS2, N5, and N6 are turned off at the same time the transistors of P7 and P8 are turned on. This phase is needed to ensure that any static current does not occur during the reset time. NS1, NS2, N5, and N6 turn on when the clock is high and P8 and P7 are simultaneously switched off.

The differential input and the latch are conducted at
the start of this phase. The differential input voltage is then changed to a differential current and is mirrored to the regenerative latch. The positive feedback on the latch changes the regeneration of a trivial differential voltage at $V_{IN}$ to a full swing differential output. After evaluating the output, the Adaptive Power Control Circuit is started. The comparator is placed in the reset phase when the clock is low. At the state of reset, the O+ and O- nodes are pulled to $V_{DD}$; the output of XOR$_1$ therefore becomes low. In this situation, the APC signals appear after the clock signal is changed. The APC signals appear when the clock is changed from 0 to 1.

The preamplifier stage changes from off to on once the APC shifts from low to high. After the comparison, the out+ (out-) shifts to $V_{DD}$ ($V_{SS}$) and the output of XOR$_1$ becomes high. Then, the APC$_1$ signal becomes high since the inputs at XOR$_2$ are high, and the APC signal finally becomes low after passing all the gates. Therefore, the power source of the comparator is turned off with the APC signal. A truth table of the outputs, the clock, and the APC signal is shown in Table 1.

Table 1. Signals state

<table>
<thead>
<tr>
<th>CLK</th>
<th>O+</th>
<th>O-</th>
<th>APC</th>
<th>STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>CLK</td>
<td>Reset</td>
</tr>
<tr>
<td>0→1</td>
<td>0</td>
<td>1</td>
<td>0→1→0</td>
<td>Evaluated</td>
</tr>
<tr>
<td>0→1</td>
<td>1</td>
<td>0</td>
<td>0→1→0</td>
<td>Evaluated</td>
</tr>
</tbody>
</table>

Table 1 shows the signals’ state of the proposed comparator circuit. The simulation result shows that the proposed design exhibits a high resolution of 13 bit and an ultra-low power consumption with 0.2 mV offset and 2.4 nsec output propagation delay.

3. Voltage Reference Generator

The schematic of the reference voltage generator is illustrated in Fig. 4. Two buffers are used to generate the reference voltages, $V_{REFT}$ (3.5 V) and $V_{REFB}$ (0.5 V), and drive the large capacitance in the DAC.

In order to meet the settling time and conversion speed, the output current of the buffer should be sufficiently large. Thus, a Class-AB type buffer is designed to simultaneously meet the requirements for low power consumption with fast settling time. The schematic of the buffer shown in Fig. 5. The internal reference voltage circuit and reference buffer will save cost and board area.

![Fig. 4. Schematic of top reference voltage generator.](image)

![Fig. 5. Class-AB type buffer used in reference voltage generator.](image)

![Fig. 6. Low-power BGR circuit used in reference voltage generator and compensation circuits in relaxation oscillator.](image)

Fig. 6 shows the new BGR used in the reference voltage generator, as well as the compensation circuits in the relaxation oscillator. A bandgap circuit is needed in order to generate a stable voltage reference with high power supply rejection ratio (PSRR) and low temperature sensitivity with supply.

This BGR must be able to completely remove the supply voltage noise at lower frequencies and maintain this ability at higher frequencies. A current mode regulator is used for isolation of the area between the supply source and the BGR circuit. A constant voltage, which is almost independent from the supply source $V_{op}$, is created to supply the BGR circuit. Because the operational amplifier (op-amp) is supplied with a voltage of $V_{DD}$, and due to the inadequacy of op-amp PSRR, a supply source ripple is initially transmitted to the op-amp,
then to $V_{\text{reg}}$. This results in incomplete independence of the reference voltage generator circuit from the supply voltage variations.

In the proposed structure, in addition to supplying the BGR circuit, the adjusted $V_{\text{reg}}$ voltage also addresses the supply of the error amplifier (op-amp) that contributes to the complete independence of the circuit from the supply source. In addition, the BGR circuit configuration has been modified to ensure ease of determining the reference voltage value and achieving a zero temperature coefficient at the desirable voltage compared to the previous configuration.

To deploy the op-amp, a two-stage amplifier is used which, in addition to supplying sufficient loop gain, has an acceptable phase margin and bandwidth. This design has $V_{\text{REF}} = 1.2 \text{ V}$ with maximum deviation of less than 3 mV at the temperature range of -40°C to 125°C. If a reference voltage of less than 1.2 V is required, we can split up the $R_4$ resistance into two smaller resistances, without imposing any other modifications, to enable the required voltage. This BGR has a -113-dB PSRR.

4. Bootstrap Switch

In most highly accurate ADCs, a bootstrapped analog switch is used for sampling. This provides a constant $R_{\text{ON}}$ by maintaining the $V_{\text{GS}}$ of the sampling switches independent of the input signals. Bootstrapped switches are utilized in the input line $V_{\text{IN}}$ and the input of CDAC to improve the linearity of the circuit because the variation of the $R_{\text{ON}}$ of the simple switches has an effect on the SFDR of the whole ADC. To reduce this effect, bootstrapped switches are used, at least for input switches. In this type of switch, the voltage of $V_{\text{GS}}$ remains unchanged as the input signal varies, thus the $R_{\text{ON}}$ remains approximately fixed, giving rise in the linearity of the circuit. The performance of the ADC at a relatively high frequency input signal is largely dependent on these switches. Fig. 7 shows a schematic of the bootstrap-switch.

5. Relaxation Oscillator

Fig. 8 shows a block diagram of the proposed relaxation oscillator. The frequency of the relaxation oscillator is determined from the current, capacitor, and supply voltage ($f_{\text{OSC}} = I/C \times V_{\text{DD}}$). By changing these three values, we obtain a different output frequency.

The external factors and temperature capacitor have a minimum effect on the supply voltage, while the amount of current change is critical to the transistor characteristic. To compensate for the minimum effect, the BGR adopts the proportional to absolute temperature (PTAT) and gain-boosting circuit to control the relaxation oscillator current, and $P_{\text{CTUNE}<1:0>}$ is added to control the effect of the process by BGR.

By adopting these two methods, the circuit generates constant frequency, regardless of the effect of temperature and process. The proposed gain-boosting circuit for temperature compensation is shown in Fig. 9(a). The internal current mirror of the gain-boosting circuit is arranged to cascade a current mirror and to minimize the effect of supply voltage variation. Fig. 9(b)
shows the operation principle of the proposed temperature compensation using PTAT. Fig. 9(b) shows that, if PTAT is not applied, the frequency varies from 23.5 MHz to 26.5 MHz. To control the current of the relaxation oscillator, the PTAT of BGR senses the temperature, and if it is relatively low, the current flow into the core increases and $V_{PTAT}$ decreases.

The changed $V_{PTAT}$ voltage compensates for the variation using the gain-boosting circuit shown in Fig. 9(a). On the other hand, if the temperature is high, the current flow into the core is reduced, and the $V_{PTAT}$ voltages increase. The changed $V_{PTAT}$ voltage compensates for the reduced current by the gain-boosting circuit. Thus, these two methods maintain a constant frequency with high accuracy.

Fig. 10(a) shows the proposed process compensation circuit. To compensate for the process variation, a voltage $V_P$ is generated, which has the least dependency on temperature and is critical to the process variation obtained by using the BGR. The role of voltage $V_P$ is to compare $V_{PREF_A}$ with $V_{PREF_B}$. The two bits signal ($P_{CTUNE}<1:0>$) generated from the comparators controls the capacitor from the capacitor bank of the relaxation oscillator core.

Fig. 10(b) shows the operation principle of the proposed process compensation circuit. When the relaxation oscillator operates without the process compensation circuit, the frequency varies from 24 MHz to 26 MHz with respect to the process variation. However, with the process compensation, the frequency is kept constant.

6. Input Buffer

A circuit schematic of the proposed top input voltage buffer amplifier is illustrated in Fig. 11. The input stage of this buffer is a differential amplifier with a bias circuit. A class-AB amplifier and its two complementary boosting transistors that implement the class-B structure are the main output parts of this circuit.

In addition, two comparators are applied in this structure. These are the current comparators which, together with M18 and M19, increase the slew rate of the output voltage. When the outputs of the comparators that are connected to the gates of the M18 and M19, are high
and low respectively, these transistors are off. Therefore, static current does not occur at the output part and the SR enhancing circuit does not increase the power consumption in the stable state.

The settling time of the amplifier consists of a slewing period and a quasi-linear period. The quasi-linear period depends on small signal behavior, while the slewing period depends on large signal behavior. As the buffer amplifier needs to derive a large capacitive load, the settling time of this amplifier is restricted by the slewing period. In a single-stage amplifier, the slew rate can be obtained as the maximum current passing through the unit load capacitance [8, 9].

The buffer amplifier is applied in unity-gain and must be able to follow the input variations. When a change occurs in the input voltage, the difference between input and output that has been feedback appears in the input of the comparators. According to the sign of this difference, one of the output transistors, either M18 or M19, is turned on, causing the load capacitor to be charged or discharged until the output voltage equals the input value. Therefore, the application of the comparators will increase the maximum charging or discharging current, which in turn will increase the slew rate and decrease the settling time of the structure.

**IV. Measurement Results**

The ADC is fabricated in a 0.18-µm CMOS technology. The micrograph of the presented ADC is shown in Fig. 12, where the active area is 0.728 mm². Fig. 13 shows the Device Under Test (DUT) and measurement setup of the 12bit ADC.

The static performance is characterized through integral nonlinearity (INL) and differential nonlinearity (DNL) measurement. The INL is the difference from absolute value and the DNL is relative difference. In successive operation, some mismatches do not reset and they are integrated. Therefore, normally, successive system by feedback has smaller DNL than that of INL. Because the error are accumulated, INL is increased. The measured INL and DNL are +2.78/-2.45 LSB and +0.36/-0.73 LSB respectively, as shown in Fig. 14.

The 65536-point (Data-Length, $2^{16}$) FFT spectrum of the proposed ADC is shown in Fig. 15, for a sinusoidal
wave inputs at 124.8 Hz and 374 kHz, respectively, sampling frequency of 750 kS/s and clock frequency of 25 MHz. The SINAD is 66.35 dB, which equates to an ENOB of 10.73 bits with 124.8 Hz input frequency and the SINAD is 64.73 dB, which equants to an ENOB of 10.46 bits with 374 kHz Nyquist input frequency. To compare the proposed ADC with other state-of-the-art SAR ADCs, the well-known figures-of-merit (FoM) equation is used [5].

\[
FOM = \frac{\text{Power}}{2^{\text{ENOB}} \times \min\{f_s, 2 \times \text{ERBW}\}}
\]

where \(f_s\) is the sampling rate and the ENOB is the effective number of bits at the effective resolution bandwidth (ERBW). The FOM of the proposed ADC is 102 fJ/conversion-step at 750 kS/s and 5.0-V supply.

As a result, the proposed dual sampling SAR ADC saves around 70% switching energy compared with conventional method. The proposed SAR ADC reduces the total capacitance by 50% \((2^{n-1} + f). C + C_{\text{S&H}}\) compared with conventional method which, the total capacitance is \(2^n C\). Also, the standard deviation of switching energy is reduced by 85% compared with conventional method.

Table 2 summarizes the measured performance of the ADC chips at room temperature. This ADC achieves a good FoM of 102 fJ/conversion-step with an ENOB of 10.73. Table 3 compares our design with some previously published ADC designs in terms of the ENOB and other metrics.

### V. CONCLUSIONS

This paper presents a 12-bit 25 MHz low power dual-sampling technique SAR ADC with reduced CDAC fabricated in 0.18-µm CMOS process technology. An energy efficient switching scheme is utilized in this design to obtain low power and high frequency operation performance. A low power dynamic latch comparator with APC and a bootstrap switch is adopted to further enhance power efficiency, and to reduce the chip area and power consumption. The results of the measurements indicate that the proposed ADC consumes 0.13 mW from a 5.0-V supply. It achieves FoM of 102 fJ/conversion-step, SINAD of 66.35 dB, and ENOB of 10.73. Actually, this technique is also applicable to SAR ADCs that operate at higher sampling frequencies.
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