A Two-Point Modulation Spread-Spectrum Clock Generator With FIR-Embedded Binary Phase Detection and 1-Bit High-Order $\Delta \Sigma$ Modulation

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Abstract—This paper describes a spread-spectrum clock generation method by utilizing a $\Delta \Sigma$ digital PLL (DPLL) which is solely based on binary phase detection and does not require a linear time-to-digital converter (TDC) or other linear digital-to-time converter (DTC) circuitry. A 1-bit high-order $\Delta \Sigma$ modulator and a hybrid finite-impulse response (FIR) filter are employed to mitigate the phase-folding problem caused by the nonlinearity of the bang-bang phase detector (BBPD). The $\Delta \Sigma$ DPLL employs a two-point modulation technique to further enhance linearity at the turning point of a triangular modulation profile. We also show that the two-point modulation is useful for the BBPLL to improve the spread-spectrum performance by suppressing the frequency deviation at the input of the BBPD, thus reducing the peak phase deviation. Based on the proposed architecture, a 3.2 GHz spread-spectrum clock generator (SSCG) is implemented in 65 nm CMOS. Experimental results show that the proposed SSCG achieves peak power reductions of 18.5 dB and 11 dB with 10 kHz and 100 kHz resolution bandwidths respectively, consuming 6.34 mW from a 1 V supply.

Index Terms—SSCG, FIR filtering, BBPLL, fractional-$N$, delta-sigma modulator, two-point modulation

I. INTRODUCTION

As the clock frequency increases, electromagnetic interference (EMI) becomes critical in high speed digital systems. Among several methods of the EMI reduction, using a spread-spectrum clock generator (SSCG) based on a $\Delta \Sigma$ PLL is considered a viable solution with full digital control and fine resolution [1-4]. The 1-bit time-to-digital converter (TDC) or the bang-bang phase detector (BBPD) enables a low-complexity digital PLL (DPLL) design and offers easy design migration from the traditional PLL by explicitly having the frequency divider. While the BBPD-based PLL (BBPLL) has been extensively used in wireline applications for clock generation and clock-and-data recovery (CDR) circuits, it could not be employed for the SSCG due to the nonlinear characteristic of bi-level phase detection. Even though spread-spectrum tracking capability is shown in the integer-$N$ BBPLL with reference clock modulation [5], the fractional-$N$ BBPLL with $\Delta \Sigma$ modulation suffers from significant bandwidth reduction and in-band noise degradation as illustrated in Fig. 1.

To overcome the nonlinear property of the BBPD and achieve good linear modulation in the $\Delta \Sigma$ PLL, a digital-to-time converter (DTC) [6] or a digital feedback to the $\Delta \Sigma$ modulator [7] is employed to minimize the phase error at the input of the BBPD. However, the use of the DTC based on the delay circuit requires nearly 10-bit
linearity for the linear modulation, and the digital feedback scheme suffers from the limited bandwidth. A multi-output BBPD along with the phase-interpolator-based fractional-N divider is proposed to perform FSK modulation with discrete frequency steps [8], but the frequency resolution is not high enough to perform linear triangular modulation for the SSCG. The SSCG based on the open-loop modulation method requires multiple fractional dividers, modulators and digital calibration circuits, which is not suitable for high frequency applications [9].

In this work, we present a BBPLL-based SSCG which does not require the linear TDC, the linear DTC, or any background calibration circuitry to achieve the linear modulation [10]. Three key techniques are employed to mitigate the phase-folding problem which is caused by nonlinearity of the BBPD: 1) adopting a high-order ΔΣ modulator with a 1-bit quantizer; 2) utilizing a hybrid FIR filter; 3) a two-point modulation technique is employed to further enhance linearity at the turning point of the triangular modulation profile [4]. We also show that the two-point modulation technique can improve the BBPLL performance by significantly reducing the frequency deviation or the peak phase deviation at the input of the BBPD [10].

The paper is organized as follows. Section II introduces linearity enhancement techniques for the ΔΣ BBPLL. Section III discusses the spread-spectrum clock generation based on the two-point modulation. Section IV describes detailed circuit implementation. Experimental results are presented in Section V, followed by conclusion in Section VI.

II. PHASE-FOLDING REDUCTION IN BBPLL

Since the BBPD provides a single-bit output, the fractional-N BBPLL cannot generate a phase error which is linearly proportional to phase variation caused by the ΔΣ modulation. As a result, a residual phase is folded at the BBPD output with a large quantization error for each reference clock period, degrading the in-band noise performance with phase detection nonlinearity [7].

1. 1-Bit High-Order ΔΣ Modulation

Fig. 2 shows a simulated nonlinear effect of the BBPD when modulation bits carrying a 1 MHz sinusoidal tone are fed to the input of the ΔΣ modulator. Spectra at the BBPD output are compared with different types of ΔΣ modulators. When a first-order MASH modulator (MASH1) is used, the spectrum shows a 1 MHz tone at the BBPD output but large spurs are observed. When a third-order MASH modulator (MASH3) is used, the spurs are reduced but the close-in phase noise becomes flat even with the high-order ΔΣ modulation. It is because the multi-phase generation by the MASH3 causes a phase folding effect with the binary phase detection, showing that the use of the high-order MASH modulators is not good for the fractional-N BBPLL. On the contrary, the spectrum with the third-order single-loop modulator (SLDSM3) exhibits a clear noise shaping effect. Hence, the high-order modulator with the 1-bit quantizer can be useful to reduce the input dynamic range without requiring the high-resolution DTC at the input of the BBPD. Since the peak frequency deviation required for the SSCG is typically in the order of 10MHz for < 5 GHz output frequency, a reference clock frequency higher than 30 MHz guarantees stability of the SLDSM3 with < 30% input dynamic range.
2. FIR-Embedded Binary Phase Detection

The hybrid FIR filtering method is useful in the fractional-N PLL to enhance the charge pump linearity and suppress the quantization noise [11]. When the hybrid FIR filter is employed for the fractional-N BBPLL, the phase folding problem due to the BBPD can be mitigated. Fig. 3 shows a block diagram of the FIR-embedded $\Delta\Sigma$ modulation with BBPDs. A $k$-tap hybrid FIR filter is realized by $k$ DFFs, $k$ dividers, and $k$ BBPDs. For each path $i$, a phase error $t_{err}$ between the reference and the divider clock ring edges is given by $t_{REF} - t_{DIV}$. Then, total phase error $\sum_{i=0}^{k} t_{err}$ for each reference clock period with the $k$-tap FIR filter is given by

\[
\text{total } t_{err} = \sum_{i=0}^{k} (t_{REF} - t_{DIV}) \tag{1}
\]

Since a random jitter due to the DCO is common for each path, only a deterministic jitter due to the $\Delta\Sigma$ modulator is considered. Then, the phase error by the $\Delta\Sigma$ quantization noise in the frequency domain is given by

\[
S_{err}(z) = \frac{(2\pi)^2}{12 f_{DSM}} \sum_{i=0}^{k} z^{-i} NTF(z) \left( \sum_{i=0}^{k} z^{-i} \right)^2 \cdot \frac{1}{N^2} \tag{2}
\]

where $NTF(z)$ is a transfer function of the quantization noise, $N$ is the division ratio, and $f_{DSM}$ is the clock frequency of the $\Delta\Sigma$ modulator, which is the same as the reference frequency.

To explain how the FIR filter mitigates the phase folding effect in the binary detection, a simplified conceptual example is shown in Fig. 4 where a 4-modulo fractional-N BBPLL with a 2-bit accumulator instead of the $\Delta\Sigma$ modulator is considered. When a dual-modulus divider $N/N+1$ is modulated by the 2-bit accumulator, an instantaneous phase error which is equivalent to one-fourth of the digitally-controlled oscillator (DCO) period $T_{DCO}$ is generated due to the periodic modulation of the dual-modulus divider for each reference clock period $T_{REF}$. Since this deterministic phase jitters (DJ) is more dominant than the random jitter mostly from the DCO, the BBPD generates UP/DN mostly from the DCO.

In Fig. 5, an instantaneous phase error and the statistical distribution of the DJ caused by $\Delta\Sigma$ modulation are compared by having the FIR filter enabled and disabled. Fig. 5(a) shows the phase error behavior without the FIR filter, which is done by having all taps synchronized. Hence, the phase error in each BBPD path from $t_{err tapped0}$ to $t_{err tapped7}$ is the same. The statistical distribution of the total phase error $\sum_{i=0}^{k} t_{err}$ at the BBPD output is plotted in Fig. 5(a). Even though the
SLDSM3 with the 1-bit output is used, phase error distribution far exceeds one DCO period due to the nonlinearity of the BBPD. On the other hand, the statistical phase error distribution with the FIR-embedded BBPDs shows much narrower distribution after all the phase errors are averaged as shown in Fig. 5(b). The results also imply that the gain of the FIR-embedded BBPDs is partially linearized thanks to the time-interleaving operation of the FIR filter.

To verify the phase folding mitigation by the 1-bit ΔΣ modulation and the hybrid FIR filtering, behavioral simulations are performed. A ΔΣ BBPLL with the fractional division ratio of about 0.41285 and the reference frequency of 60 MHz is run to generate the output frequency of about 3.025 GHz. To maintain the same loop gain between the 8-tap FIR and the non-FIR modes, all eight frequency dividers are modulated by one output of the ΔΣ modulator for the non-FIR mode instead of changing the DLF. Fig. 6(a) shows transient settling behaviors of loop control words with the MASH3, the FIR-embedded MASH3, the SLDSM3, and the FIR-embedded SLDSM3. As seen in Fig. 6(a), the ΔΣ BBPLL with the SLDSM3 exhibits slightly less ringing than that with the MASH3, and the ΔΣ BBPLLs with FIR-embedded modulators achieve less voltage ripples with good suppression of the DJ which is caused by the ΔΣ modulator. Fig. 6(b) shows phase noise performance. The ΔΣ BBPLL with the SLDSM3 achieves better in-band noise performance, and it is further improved when the FIR filter is used. It is found that the in-band noise suppression performance by the hybrid FIR filter achieves better performance when the ΔΣ modulator is clocked by the third of fourth divider output rather than the first divider output, showing that the phase folding effect depends on the phase offset condition. The simulation results also show that the fractional spur performance is significantly improved with the FIR filter.

III. SSCG WITH TWO-POINT MODULATION

The SSCG based on the ΔΣ PLL is shown in Fig. 7 provides an accurate control of modulation with fine resolution. Since the triangular modulation is achieved by modulating the frequency divider only, the PLL works as a low-pass filter to this one-point modulation. Accordingly, the PLL bandwidth needs to be much higher than the modulation frequency to provide a sharp tuning point with the triangular modulation. When the
Wide bandwidth is designed, the ΔΣ PLL suffers from short-term jitter due to the increased high frequency quantization noise. A Hershey-Kiss or other complex modulation profile [3] could be considered but it requires additional design effort with nonlinear modulation profile, which may not be effective with the nonlinear loop dynamics of the BBPLL.

On the other hand, the two-point modulation method shown in Fig. 8 overcomes the bandwidth control problem by having two modulation paths. The high-pass transfer characteristic of the DCO modulation and the complementary low-pass transfer characteristic of the frequency divider modulation form an all-pass transfer function regardless of the PLL bandwidth. Hence, the PLL bandwidth can be optimized for other performances. The two-point modulation, however, suffers from the gain mismatch and DCO nonlinearity [4]. Several methods regarding the gain calibration are proposed, including the just-in-time algorithm [12], the consecutive counting operation [13], and the least-mean-square (LMS) based gain calibration [14]. However, the gain mismatch can be calibrated by digital compensation as shown in the recent two-point modulation SSCG with the BBPD [15], the DCO nonlinearity could be problematic. Since the frequency deviation of the SSCG is not high compared to the output frequency, the use of the separate FIR-embedded 1-bit ΔΣ modulation only for the high-pass modulation path can be considered as a future work [16]. In this design, the initial DCO gain mismatch calibration is manually done by the field programmable gated array (FPGA). In the calibration, we set the digital varactor control words to be 0 or 1, to detect the DCO gain. The measurement results show that the DCO gain of 248 kHz/bit with the frequency modulation of 31.7 MHz is obtained.

Another benefit of using the two-point modulation for the SSCG is illustrated in Fig. 8. In the two-point modulation, the role of the fractional-N divider is to cancel the low frequency component of the DCO modulation, so that the modulation signal MOD_H at the DCO input is not high-pass filtered in the PLL. Since the modulation frequency is within the PLL bandwidth, the fractional-N divider modulated by the ΔΣ modulator should completely cancel the spread-spectrum signal with the modulation signal MOD_L as depicted in Fig. 8. As a result, the use of the two-point modulation is helpful for the BBPLL based SSCG since the large frequency deviation by the triangular modulation profile is not seen at the input of the BBPD, thus significantly reducing the phase folding effect.

In Fig. 9, transient control voltages of the conventional charge pump PLL with the bandwidth of 1 MHz are compared to those of the BBPLL. The hybrid FIR filter is not used in the simulation. For clear comparison, the charge pump and the passive loop filter are also used for the BBPLL. The control voltage at the capacitor $V_C$ and the VCO input $V_{CTR}$ are plotted to show the frequency deviation and the phase error respectively. As expected, the frequency deviation is constant and the peak phase deviation is significantly suppressed in the two-point modulation. As for the BBPLL, the peak phase deviation is less suppressed than that of the analog PLL, while the frequency deviation is nearly constant.

To verify the proposed SSCG architecture having the hybrid FIR filter, behavior simulations are performed with MATLAB software for fast simulation. As shown in Fig. 10(a) and (b), both the one-point modulation and the two-point modulation show the similar performance, but the control voltage of the VCO with the two-point modulation shows better linearity. The fractional spur at 20 MHz offset is observed at 3.2 GHz output with the

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**Fig. 7.** SSCG with one-point modulation.

**Fig. 8.** SSCG with two-point modulation.
reference frequency of 60 MHz. The clock spectrum in the two-point modulation is more suppressed by about 2 dB than that in the one-point modulation. The simulation results clearly show that the two-point modulation is helpful to improve the SSCG performance even if the PLL bandwidth is sufficiently wide enough to track the triangular modulation profile.

IV. CIRCUIT DESIGN

Fig. 11 shows a block diagram of the proposed SSCG based on the BBPLL and the 8-tap hybrid FIR filter. Since the open-loop gain of the BBPLL is significantly reduced with the fractional-N mode [7], the gain of each BBPD is not scaled by 8 in the FIR filtering mode to compensate for the reduced open-loop gain during the fractional-N mode. To achieve good linearity of triangular modulation, two-point modulation is done by utilizing both high-pass modulation and low-pass modulation paths as discussed previously. In addition, a spread-spectrum insensitive jitter monitor is designed to extract the jitter transfer function of the BBPLL. The SSIJM consists of an analog delay-locked loop (DLL) with > 50 kHz bandwidth, a coarse phase rotator, and a sub-ranging 1-bit ΔΣ TDC. The DLL suppresses the periodic jitter by the 30 kHz modulation and generates the multi-phase signals to the coarse-tracking phase rotator. The selected two phases become two-level reference phase for the 1-bit ΔΣ TDC that performs the fine phase tracking with oversampling [14-17].

Fig. 12 shows a schematic of the DCO. The input of the DCO consists of a 128-bit thermometer-coded control word for fine tuning and seven binary-coded control bits for coarse tuning. To achieve good power efficiency, a current bias and a cross-coupled pair are designed with NMOS transistors. The resistor R1 and the capacitor C1
form a low pass filter in the bias current. The fine frequency step of 258 kHz is designed with the 128-bit thermometer code. Having a differential spiral inductor of 3.2 nH, the DCO achieves the tuning range of 2.7-to-3.5 GHz and consumes 2.01 mW from a 1 V supply.

The diagram of the proposed SLDSM3 with a 1-bit quantizer is shown in Fig. 13(a). It consists of three integrators and a 1-bit quantizer followed by three feedback loops. The parameters of a0-a2 and b1 are designed to be 1, 4, 4, and 4 to make the modulator stable over the required input range. Fig. 13(b) demonstrates the spectrum output of the modulator with a constant input. It clearly shows the 60 dB/dec slope of the noise shaping. To satisfy the stable requirement, the input range from 0.2 to 0.8 is able to be used which is wide enough for the SSCG modulation.

V. MEASUREMENT RESULTS

A prototype 3.2 GHz BBPLL is implemented in 65 nm CMOS. Fig. 14 shows a chip micrograph. The die area including PADs is 1.0 mm x 1.45 mm, and the active area of the BBPLL is 0.271 mm². The 3.2 GHz SSCG consumes 6.34 mW from a 1 V supply.

The measured phase noise performance at 3.2 GHz output with different modulation modes is shown in Fig. 15. The division ratio of 53.33 with the reference frequency of 60 MHz is used. The in-band noise performance with the SLDSM3 is improved by nearly 15 dB than that with the MASH3. When the 8-tap FIR filter is enabled, the bandwidth of the BBPLL is reduced even with 8 times the PD gain as expected from previous discussion. The results prove that the FIR-embedded binary phase detection helps to linearize the loop dynamics of the BBPLL. The measured integrated phase error from 1 MHz to 100 MHz, or the short-term jitter is 2.96 ps rms at 3.2 GHz output. Fig. 16 shows the measured...
output spectrum with the SLDSM3. With the FIR filter, high frequency noise is reduced by 18 dB, resulting in improved short-term jitter performance. The fractional spur at 20 MHz offset frequency is also suppressed to < –40 dBc when the FIR filter is enabled. The reference spur is –62 dBc which is not affected by the FIR filter.

Fig. 17 shows the measured SSCG spectrum. The modulation frequency of 30 kHz and the frequency deviation of –5000 ppm which is about 16 MHz are used. With the proposed simple DPLL architecture, peak power reductions of 18.5 dB and 11 dB are achieved with resolution bandwidths of 10 kHz and 100 kHz respectively. Based on the simulation results, the EMI reduction of > 16 dB can be achieved with the resolution bandwidth of 100 kHz when better frequency modulation profiles such as the Hershey-kiss profile are employed.

The measured frequency modulation waveform in time domain is shown in Fig. 18 in which the measured triangular modulation profiles are compared with the one-point and the two-point modulations. The DCO modulation path compensates the divider modulation path, which proves that the bandwidth is reduced by the FIR filtering. Table 1 gives the performance summary of this work.

**Table 1. Performance Summary**

<table>
<thead>
<tr>
<th>Performance Summary</th>
<th>65nm CMOS</th>
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<tbody>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.0V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>7.14mW</td>
</tr>
<tr>
<td>DCO</td>
<td>2.01mW</td>
</tr>
<tr>
<td>Digital Blocks</td>
<td>2.42mW</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.271mm²</td>
</tr>
<tr>
<td>DCO output Frequency</td>
<td>2.7–3.50Hz</td>
</tr>
<tr>
<td>Reference Clock</td>
<td>60MHz</td>
</tr>
<tr>
<td>Phase Noise @ 1MHz</td>
<td>-95dBc/Hz</td>
</tr>
<tr>
<td>Reference Spur</td>
<td>-62dBc</td>
</tr>
<tr>
<td>RMS Jitter</td>
<td>2.96ps</td>
</tr>
<tr>
<td>Measured EMI reduction</td>
<td>18.5dB @ 10kHz RBW (30kHz Triangular)</td>
</tr>
<tr>
<td></td>
<td>11dB @ 100kHz RBW</td>
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**VI. CONCLUSION**

A 3.2 GHz SSCG based on a BBPLL which does not require linear TDC or DTC circuitry is implemented in 65 nm CMOS. This work shows that the genuine BBPD can be used for the SSCG with the decent short-term jitter performance by utilizing the hybrid FIR filtering and the 1-bit high-order ΔΣ modulation techniques. It is also shown that the two-point modulation is useful for
the SSCG to improve the spread-spectrum performance by significantly reducing the peak frequency deviation at the input of the BBPD, thus reducing the phase deviation. Experimental results show that peak power reductions of 18.5 dB and 11 dB are achieved with 10 kHz and 100 kHz resolution bandwidths respectively. Having good immunity to circuit nonlinearity, the proposed architecture is highly useful for low-complexity modulation systems including ultra-low voltage applications.

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