Design and Evaluation of a CMOS Image Sensor with Dual-CDS and Column-parallel SS-ADCs

Bu-Yong Um\textsuperscript{1}, Jong-Ryul Kim\textsuperscript{1}, Sang-Hoon Kim\textsuperscript{1}, Jae-Hoon Lee\textsuperscript{1}, Jimin Cheon\textsuperscript{2}, Jaehyuk Choi\textsuperscript{2}, and Jung-Hoon Chun\textsuperscript{1}

Abstract—This paper describes a CMOS image sensor (CIS) with dual correlated double sampling (CDS) and column-parallel analog-to-digital converter (ADC) and its measurement method using a field-programmable gate array (FPGA) integrated module. The CIS is composed of a 320 x 240 pixel array with 3.2 \( \mu \)m x 3.2 \( \mu \)m pixels and column-parallel 10-bit single-slope ADCs. It is fabricated in a 0.11-\( \mu \)m CIS process, and consumes 49.2 mW from 1.5 V and 3.3 V power supplies while operating at 6.25 MHz. The measured dynamic range is 53.72 dB, and the total and column fixed pattern noise in a dark condition are 0.10\% and 0.029\%. The maximum integral nonlinearity and the differential nonlinearity of the ADC are +1.15 / -1.74 LSB and +0.63 / -0.56 LSB, respectively.

Index Terms—CMOS image sensor, CIS, dual CDS, single-slope ADC, fixed pattern noise

I. INTRODUCTION

Fixed pattern noise (FPN) is the most important factor in determining the quality of the images captured by CMOS image sensors (CIS). According to noise sources, FPN is categorized into pixel FPN and column FPN. The pixel FPN arises from dark current in pixels and mismatches of pixel transistors, especially threshold voltage difference between source follower transistors. In the column-parallel architecture, the comparator offset in each column results in the column FPN. Correlated double sampling (CDS) has been widely employed to reduce FPN due to mismatches of columns and transistors [1-5]. There are three types of CDS: analog CDS using the capacitors and switches in front of an analog-to-digital converter (ADC) [2, 3], digital CDS with double counting of reset and readout signals [4], and dual CDS which employs both analog and digital CDS schemes [5]. The digital CDS suppresses FPN more precisely than the analog CDS, although it requires additional analog-to-digital conversion time for sensing the reset voltage. The dual CDS compensates for the drawback of the digital CDS by employing the analog CDS.

Because image sensors for mobile applications need a small area and low power consumption, the column-parallel architecture satisfying these conditions has been prevalently employed [4-6]. In the column-parallel architecture, the simple single-slope ADC (SS-ADC) is preferred, because it can fit in a pixel pitch or two. In this paper, we demonstrate a dual-CDS CIS with column-parallel ADCs including double-data rate counters that utilize rising and falling edges of an operating clock to reduce power consumption [7]. We have also implemented a test system with a field-programmable gate array (FPGA) integrated module, which generates control signals for the CIS and converts sensor output signals to an image, performs systematic measurements, and quantify the image quality with proper performance metrics [8].

Section II provides the principle of the dual CDS...
scheme, the architecture of the implemented CIS system, and the details of the core circuits. The CIS evaluation method and the measurement results are presented in Section III, followed by the conclusion in Section IV.

II. DUAL-CDS CIS SYSTEM

1. Single-Slope ADC with Dual CDS

Fig. 1 shows the simplified block diagram of the SS-ADC that can perform dual CDS. The output of the pixel is connected to one input of the comparator. A ramp signal that comes from an external ramp generator is connected to the other input of the comparator. These two signals pass through capacitors to perform dual CDS. The control signals provided by the FPGA determine the operation modes of the 10-bit up/down counter. The pixel’s analog voltage is finally converted to the 10-bit digital codes, D[0]–D[9].

Fig. 2 is the dual-CDS timing diagram of the SS-ADC. The Row_sel signal selects a row for a read operation. The Row_sel is maintained at ‘1’ while the output of the pixel is connected to the comparator and the A/D conversion for a row is accomplished through the following five steps. The first step, step (1) in Fig. 2, is ‘reset sampling.’ The Pixel_rst signal is applied and the pixel reset voltage is transmitted to the capacitor of the comparator. In the second ‘comparator reset’ step, the Comp_rst becomes high, and the inputs and the outputs of the comparator are set to the same reset level. In step (2), one side of the capacitor connected to the pixel is set to the pixel reset voltage, while the other side is set to the comparator reset voltage. Step (3) is ‘down-counting.’ The Comp_rst signal turns off the reset switches of the comparator. The ramp signal rises up instantaneously by 256 codes and then falls down slowly by 384 codes. At this time, the counter starts down-counting until the ramp signal becomes equal to the reset voltage of the comparator. Therefore, the counter holds the digitized reset voltage of the comparator. This digitized reset value can be different across the rows because of random offsets of the comparators. Next is step (4), ‘signal sampling.’ As the Tx signal is applied, electrons from the photodiode cause a voltage drop at the output node of the pixel according to light intensity. Since the output of the photodiode and the comparator are AC coupled, only the signal voltage of the photodiode (= pixel reset voltage – photodiode voltage) is transmitted to the comparator input. This analog CDS scheme suppresses pixel FPN from the offset variation of in-pixel circuits. Finally, step (5) is ‘up-counting.’ In this step, the ramp signal instantaneously rises up again and falls down slowly by 1536 codes. During the second ramping period, the counter starts up-counting until the ramp signal reaches the other input signal (= comparator reset voltage + photodiode signal voltage). By subtracting the Count_out from step (3) from the Count_out from step (5), we can get the digitized signal strength. It should be noted that this digital CDS scheme with successive down- and up-counting sequences effectively eliminates the offsets between the comparators. In this way, the dual CDS scheme cancels the column FPN form the digital CDS as well as the pixel FPN from the analog CDS, which enhances image quality by suppressing overall FPN.
2. CIS System Architecture

Fig. 3 shows the entire structure of the implemented dual-CDS CIS system that consists of a sensor chip and a characterization module. The sensor chip includes a 320 × 240 pixel array (QVGA) and column-parallel single-slope ADCs, while the characterization module has a ramp generator and an FPGA for operation control and signal processing. Each column of the pixel array is connected to a readout circuit composed of a comparator, an up/down counter, an SRAM, and a sampler. The column and row scanners are shift registers that receive control signals from the FPGA to determine which A/D conversion results are sent to the FPGA module. The off-chip ramp generator supplies the ramp signal for the comparators. The control signal generation block inside the FPGA module generates a clock for the counter and various control signals that drive the CIS and the ramp generator. The even and odd column data from the CIS are first merged by the multiplexers, then are transmitted to an external computer through the FPGA-USB interface block, and finally are converted to digital images.

Fig. 4 shows Verilog simulation results of the control signals indicated in Fig. 3. The control signal generation block has a finite state machine with 14 states in total, which are categorized and simplified in Fig. 4. Every control signal is synchronized with a main clock so that the operating frequency can be easily controlled. In the ‘Vsync’ state, the Vsync initializes the address of the FIFO between the FPGA and the USB microcontroller to read a new frame from the CIS. Then, the control signals for the row scanner (Row_clkn, Pixel_rstn, Txn) are generated to skip dummy rows in the ‘Preset’ state. In the third state, ‘Reset Count,’ a row of the pixel array is selected, and the pixels and the comparators of the selected row are reset. Then, the comparator reset voltage is down-counted as shown in step (2) of Fig. 2. In the next ‘Signal Count’ state, the Txn is applied to read the voltage induced by the incident light in each pixel. The light-induced voltage is up-counted and held by the counter. Finally, the digitized signal values from the counter are stored in the SRAM and are transmitted to the interface block through the samplers in the ‘SRAM Read’ state. The process from the ‘Reset Count’ state to the ‘SRAM Read’ state is repeated 240 times to construct a full QVGA image.

3. Circuit Implementation

The structure of the comparator as implemented is shown in Fig. 5(a). The comparator is composed of a simple differential amplifier with a single-ended output and a self-biased common source amplifier [9]. The analog CDS is performed by the capacitors at the inputs and the reset switches between the input and the output of the first stage. The bias current of the first stage is only 3 μA for low power consumption, so the current source is cascoded to reduce noise from the bias circuit. The second gain stage offers an additional gain with limited power consumption. When the Comp_rst is high, the inputs and the outputs of the first stage are connected and set to the same reset level. At the same time, the second stage is biased with half of the first stage’s bias.
current (because $M_{P1}$, $M_{P2}$, and $M_{P3}$ are identical), while the NMOS transistor of the second stage, $M_{N5}$, is accordingly biased. When the Comp_rst becomes low and the comparator begins to compare Ramp and Pixel_out, the capacitor of the second stage maintains the gate voltage of $M_{N5}$ so that the second stage is still appropriately biased and provides a significant gain. Fig. 5(b) shows how much current is saved as we adopt a self-biased common-source amplifier for the second stage, instead of a simple inverter. Because the ramp signal (INN of the 1st stage) changes with a regulated slope, the output voltage of the first stage transits slowly. If the second stage were a simple inverter, it could have a large dynamic current. However, the self-biased amplifier maintains the low bias current under this condition.

The ground of the first stage is separated from that of the second stage using a deep n-well to reduce the susceptibility to ground noise. The total gain of the comparator is 72 dB, while the first stage has a 36-dB gain.

Fig. 6 describes the structure of the double data rate up/down counter [7] that is driven by the comparator output, Comp_out, and the counter clock, Counter_clk. The counter performs the digital CDS with sequential processes: down-counting, holding an intermediate result, and up-counting. The FPGA provides the control signals (i.e., Counter_en, RST, UD, and HLD). The UD signal determines the up/down counting mode. When the HLD is high, the counter maintains current outputs. The counter has a 10-bit output, $D[0-9]$, while $D[0]$ is the least significant bit (LSB). $D[0']$ and $D[1]$ are toggled at the rising edges and the falling edges of the clock, respectively. However, $D[0]$ can be changed at both edges of the clock because it is obtained by XORing $D[0']$ and $D[1]$. Therefore, the operating clock frequency for the counter is halved, while the power consumption is reduced accordingly. The power consumption can further be reduced by avoiding unnecessary toggling of $D[0]$. That is, $D[0]$ is toggled only when the up/down counting mode is changed, or the counter output is stored in the SRAM. When the counting mode is changed from down-counting to up-counting, $D[0]$ value is required since $D[0]$ determines whether the Clk starts from a rising edge or a falling edge in up-counting mode. As illustrated in Fig. 7(a), if $D[0]$ is zero when the down-counting is finished, only $D[0]$ should be toggled, while the other nine bits should be maintained when the up-counting begins. Therefore, the up-counting mode begins at a rising edge of the Clk and $D[0]$ is toggled by $D[0']$. In the other case, $D[0]$ must be toggled by $D[1]$, so the Clk
starts from a falling edge in the up-counting mode as shown in Fig. 7(b). This double data rate counter in a column consumes 2.28 μW, which is about a half comparing with the power consumption of a single data rate counter (4.4 μW).

The post-layout simulation results of the single-slope ADC are shown in Fig. 8. The Counter_out represents the 10-bit output of the counter as decimal numbers. In this simulation, the reset voltage of the pixel is 2.8 V and the photodiode voltage after light exposure is 2.4 V. That is, the signal voltage is 0.4 V. If the maximum signal voltage is 1 V, the theoretical A/D conversion result is 0110011010 (=410_{10}). As shown in Fig. 8, when the Ramp crosses the Pixel_out signal, the Comp_out is flipped and the Counter_out is fixed. The final output of the counter matches the theoretical value.

### III. CIS Evaluation Method and Measurement Results

#### 1. Test Environment Implementation

The CIS chip is fabricated in a 0.11-μm CIS process and bonded on the daughterboard, as shown in Fig. 9(a) and (b). The QVGA pixel array includes dummy columns and rows for monitoring internal nodes and characterizing the ADCs with a test input. The size of the CIS core is 2090 μm × 1780 μm. Fig. 9(c) shows the layout of two comparators and two 1-bit sections of the...

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**Fig. 7.** Timing diagrams of the counter (a) when \( D[0] = 0 \), (b) when \( D[0] = 1 \) after down counting.

**Fig. 8.** Simulation result of the single-slope ADC.

**Fig. 9.** (a) Microphotograph of the fabricated chip, (b) COB bonded chip on the daughterboard, (c) layout of a part of two columns.
Because the CIS in this paper employs a column-parallel ADC structure and has readout circuits placed on both sides of the pixel array, the pitch of a readout circuit is twice the pixel pitch. Any mismatches between the differential paths of the comparator affect conversion results significantly because the step of the ramp signal is less than 1 mV. Therefore, placement and routing of the transistors and the capacitors strictly conform to the symmetry. The counter circuits reside in a deep n-well to minimize noise injections to the analog domain.

Fig. 10 illustrates the block diagram of the CIS test environment, which consists of a daughterboard, a motherboard, and software. The daughterboard including the CIS chip stands perpendicular to the motherboard to capture a subject in a horizontal position. The motherboard contains an FPGA integrated module [10] and a ramp signal / test input generator. The ramp signal generator for the single-slope ADC is composed of a digital-to-analog converter (DAC) and an operational amp (OP-amp). The arbitrary test input directly connected to the ADC input is generated by the same structure with the ramp generator. The PLL on the FPGA module provides clocks to an FPGA and a USB microcontroller. The CIS output data are transmitted to the USB microcontroller via a FIFO because the frequency of the USB interface clock and that of the CIS clock are different. Then, the data are transferred to an external computer through a USB port and are displayed as an image by the software. The software is implemented based on an API supported by an FPGA module vendor [11], and controls the frequency of the clocks from the PLL in real time. Fig. 11(a) shows the manufactured motherboard with the FPGA module and the ramp signal / test input generator. The FPGA module is located at the top of the board and the generators are on both sides. At the bottom, the daughterboard with the CIS chip and a lens is connected by a DIN connector. The CIS evaluation board in Fig. 11(b) is a combination of the two boards.

The ramp signal / test input generator on the motherboard converts the digital outputs of the FPGA to analog signals. As shown in the schematic of Fig. 12(a), the DAC generates differential current outputs depending on the codes of the FPGA, and the OP-amp changes them to a single-ended voltage [12]. The resistor values around the OP-amp are determined to support the swing range of 1.45–2.95 V and the voltage step of 1/1024 V. Fig. 12(b) presents the measurement result of the ramp signal generator. The ramp signal repeats itself periodically for the ADC to convert the rows of the pixel array in order. It has the slope of 12.2 V/ms when the CIS operates at 6.25 MHz. The generator can operate at 150 MHz maximum and has a settling time of 20 ns when it produces a 1.2-V step signal.

2. Measurement of Characteristics

Fig. 13 presents the captured digital images obtained from the CIS system as implemented. Whether an image is taken from lower 8 bits or higher 8 bits (out of 10-bit data) is selected by a switch. Obviously, the lower 8-bit image in Fig. 13(a) presents dark regions better than the
higher 8-bit image in Fig. 13(b). However, the extremely bright regions reveal the details only in the higher 8-bit image. The CIS chip consumes 49.2 mW operating at 6.25 MHz, while the pixel array consumes 26.4 mW.

The performance metrics of the CIS were extracted from the captured images based on the Standard Mobile Imaging Architecture (SMIA) standard [8]. The dynamic range is an illumination range that an image sensor can represent in a frame; it is calculated as the full-scale deflection (FSD) divided by the standard deviation of the noise. The FSD is defined as the actual pixel output range, and the standard deviation of the noise is obtained from every pixel output of an image captured in a dark condition. To measure the FPN, we first take 50 images with dark illumination and average them out to remove temporal noise. The column FPN is the RMS value of the differences between adjacent columns, and the total FPN is calculated as the spatial standard deviation of the mean image. Therefore, the total FPN at dark is expressed as follows:

$$\text{FPN} (%) = \frac{1}{FSD} \sqrt{\frac{1}{MN} \sum_{i=0}^{N-1} \sum_{j=0}^{M-1} (P_{ij} - \bar{P}_{ij})^2}$$  \hspace{1cm} (1)$$

where M and N are the total number of columns and rows respectively, $P_{ij}$ is the pixel output of $i$th column and $j$th row in the mean image, and $\bar{P}_{ij}$ is the average of all the pixel outputs of the mean image. The measured dynamic range, the total FPN, and the column FPN are 53.72 dB, 0.10%, and 0.029%, respectively.

Fig. 14(a) and (b) show the mean images generated from captured images in a dark condition using the analog CDS scheme only and the dual CDS scheme, respectively. Both are digitally quadrupled for clear comparison. Vertical noise lines appear clearly in Fig. 14(a) because the digital CDS which is supposed to
reduce the comparator offsets in each column is not activated. The total FPN and the column FPN calculated from the image in Fig. 14(a) are 0.27% and 0.34% respectively, which are much larger than the previous numbers.

The column parallel ADCs were characterized using the aforementioned test column. In the test mode, the test column receives the test input instead of a pixel output. The FPGA increases the test input from the minimum code to the maximum code at every frame, and the test column data (which are ignored in the normal operation mode) are now processed by the software. The outputs of each test column in a frame are averaged out to remove temporal noise. Then, the INL and the DNL are extracted from the mean output values. Fig. 15 shows that the analog-to-digital conversion results of the test column ADC successfully reconstruct the ideal test inputs. The INL and DNL profiles of the test ADC are shown in Fig. 16. The maximum INL in 10–90% codes is +1.15 / -1.74 LSB and the maximum DNL is +0.63 / -0.56 LSB.

Table 1. Performance comparison table

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<th>[2]</th>
<th>[13]</th>
<th>This work</th>
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<td>0.13 μm</td>
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<td>5.6 × 5.6</td>
<td>3.2 × 3.2</td>
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<td>320 × 240</td>
<td>640 × 480</td>
<td>320 × 240</td>
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<tr>
<td>ADC Type</td>
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<td>Logarithmic SS ADC</td>
<td>Three step SS ADC</td>
<td>SS ADC</td>
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<tr>
<td>CDS Type</td>
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<td>Analog Analog</td>
<td>Dual</td>
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<td>ADC Resolution</td>
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<td>10 bit</td>
<td>12 bit</td>
<td>10 bit</td>
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<tr>
<td>Column FPN</td>
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<td>0.046%</td>
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<tr>
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<td>37 fps</td>
<td>200 fps</td>
<td>20 fps</td>
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<tr>
<td>Dynamic Range</td>
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<td>80 dB</td>
<td>N/A</td>
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<td>Power Consumption</td>
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<td>76 mW</td>
<td>49.2 mW</td>
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Table 2. Performance summary (measurements)

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<tbody>
<tr>
<td>Process</td>
<td>2090 μm × 1780 μm</td>
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<tr>
<td>Pixel Size</td>
<td>3.2 μm × 3.2 μm</td>
</tr>
<tr>
<td>Array Format</td>
<td>320 × 240 (QVGA)</td>
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<tr>
<td>ADC Resolution</td>
<td>10 bit</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>6.25 MHz (max)</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>53.72 dB</td>
</tr>
<tr>
<td>Total FPN</td>
<td>0.10%</td>
</tr>
<tr>
<td>Column FPN</td>
<td>0.029%</td>
</tr>
<tr>
<td>Max INL (10-90%)</td>
<td>+1.15 / -1.74 LSB</td>
</tr>
<tr>
<td>Max DNL</td>
<td>+0.63 / -0.56 LSB</td>
</tr>
<tr>
<td>Power Supply</td>
<td>3.3 V / 1.5 V</td>
</tr>
<tr>
<td>Total / Pixel Power Consumption</td>
<td>49.2 / 26.4 mW</td>
</tr>
</tbody>
</table>

Table 1 summarizes the performance of this work and prior arts. The demonstrated CIS has lower column FPN than other CISs because the dual CDS effectively reduces FPN. The performances of the ADC and the CIS system are summarized in Table 2.

IV. CONCLUSIONS

A dual-CDS CIS with 10-bit single-slope ADCs is successfully demonstrated using 0.11-μm CIS technology. Performing the analog/digital dual CDS scheme, the CIS with a 320 × 240 pixel array successfully removes the offsets of each pixel and column. The counter of the ADC utilizes the double data-rate scheme to reduce power consumption, and the overall CIS consumes a total power of 49.2 mW, including a pixel power of 26.4 mW when operating at 6.25 MHz. The CIS measurement method using an FPGA integrated module was demonstrated. The
FPGA module generates driving signals of the CIS and visualizes the output data as a digital image. The performance of the CIS was evaluated in compliance with the SMIA standard; the assessed dynamic range, total FPN, and column FPN in a dark condition were 53.72 dB, 0.10%, and 0.029%, respectively. The column-parallel ADCs were characterized automatically by utilizing a test column receiving a comparator input from the FPGA. The maximum INL in 10–90% codes and the maximum DNL were +1.15 / -1.74 LSB and +0.63 / -0.56 LSB, respectively.

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Bu-Yong Um received the B.S. and M.S. degrees in Semiconductor system engineering from Sungkyunkwan University, Korea, in 2014 and 2016, respectively. In 2016, he joined Samsung Electronics, Korea, where he has been working on the design of CMOS image sensors for automotive applications. His research interests include CMOS image sensors and high-speed serial interface.

Jong-Ryul Kim received the B.S. degree in Semiconductor system engineering from Sungkyunkwan University, Korea, in 2014 and the M.S. degree at the same university, in 2016. He is currently assistant engineer of next-generation memory part at Samsung, Korea. His research interests include analog, digital circuit design and CMOS imager system.
Sang-Hoon Kim received the B.S degree in Semiconductor system engineering from Sungkyunkwan University, Korea, in 2013. He is currently pursuing the Ph.D. degree at the same university. His research interests include analog, digital circuit design for low-power and high-speed serial links and CMOS imager system.

Jae-Hoon Lee received the B.S degree in Semiconductor system engineering from Sungkyunkwan University, Korea, in 2015. In 2015, he joined the RF development team, Samsung, Korea, where he has been working on high speed analog to digital converter for wireless communication systems. His research interests include analog to digital converter.

Jimin Cheon received the B.S., M.S., and Ph.D degrees in electrical and electronic engineering from Yonsei University, Seoul, Korea in 2003, 2005 and 2010, respectively. From 2010 to 2012, he was a senior engineer with the Image Development Team of System LSI Division at Samsung Electronics, Yongin, Korea working on the design of APS-C CMOS image sensors for mirrorless and DSLR cameras. From 2012 to 2013, he was a manager with the Semiconductor Tech. Laboratory of Fusion Technology R&D Center at SK telecom, Seongnam, Korea working on the design of automotive CMOS image sensors with SK hynix. In 2013, he joined Kumoh National Institute of Technology, Gumi, Korea as an assistant professor in the school of electronic engineering. His research interests include CMOS image sensors, low-power data converters, high performance sensors and interface circuits.

Jaehyuk Choi received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 2004; the M.S. degree in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2006; the M.S. degree in electrical and computer engineering from the University of Minnesota, Minneapolis, MN, USA, in 2008; and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA in 2013. From 2013 to 2016, he was a research staff member with Samsung Advanced Institute of Technology (SAIT), Samsung Electronics, Suwon, Korea, where he engaged in researching depth sensors and low power image sensors. In 2016, he joined the Department of Semiconductor Systems Engineering, Sungkyunkwan University, Suwon, Korea, as an Assistant Professor. His research interests include low power circuits, CMOS sensors, and mixed-signal integrated circuits.

Jung-Hoon Chun is an Associate Professor at Sungkyunkwan University, Korea. He received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Korea, in 1998 and 2000, respectively. In 2006, he received the Ph.D. degree in electrical engineering from Stanford University. From 2000 to 2001, he worked at Samsung Electronics where he developed BiCMOS RF front-end IC for wireless communication. From 2006 to 2008, he was with Rambus Inc. where he worked on high-speed serial interfaces such as FlexIO, XDRTM, XDR2TM etc. Dr. Chun also consults for several IC design and foundry companies in Korea and Silicon Valley. His current research includes high-speed serial link, image sensors, on-chip ESD protection and I/O design, new memory devices, etc.