This paper reports on our investigation of DC and RF characteristics of p-channel metal oxide semiconductor field effect transistors (pMOSFETs) with a compressively strained Si$_{0.8}$Ge$_{0.2}$ channel. Because of enhanced hole mobility in the Si$_{0.8}$Ge$_{0.2}$ buried layer, the Si$_{0.8}$Ge$_{0.2}$ pMOSFET showed improved DC and RF characteristics. We demonstrate that the $1/f$ noise in the Si$_{0.8}$Ge$_{0.2}$ pMOSFET was much lower than that in the all-Si counterpart, regardless of gate-oxide degradation by electrical stress. These results suggest that the Si$_{0.8}$Ge$_{0.2}$ pMOSFET is suitable for RF applications that require high speed and low $1/f$ noise.

I. Introduction

Improvements in the operating speed in complementary metal oxide semiconductor (CMOS) field effect transistors (FETs) have been accomplished by reducing the channel length and gate oxide thickness [1]. However, the performance of p-channel MOSFETs remains inferior to that of n-channel MOSFETs because the hole mobility is much lower than the electron mobility [2]. Recently, the introduction of a strained SiGe layer into a pMOSFET has been receiving a great deal of attention because holes can transport faster in the SiGe channel. This is because there is larger hole mobility in compressively strained SiGe layers than that in unstrained Si layers. The confinement of holes in a SiGe buried channel, which separates carriers from the gate oxide interface where the carrier transport is hindered by scattering, also improves the carrier transport [3]. In addition, the SiGe device has shown an improved $1/f$ noise characteristic, which is particularly important in RF applications [4], [5]. The $1/f$ noise causes unwanted phase noise in mixers and oscillators [6]. In fact, the $1/f$ noise is critical in deep submicron MOSFETs, because the noise level is inversely proportional to the product of gate length (L) and gate width (W) [7]. Nevertheless, the RF potential in SiGe pMOSFETs has been rarely investigated, despite the growing attention of CMOS devices towards RF applications [1], [8].

In our investigation, we fabricated both SiGe and all-Si pMOSFETs and studied their DC and RF characteristics. Among the RF parameters, we emphasize the $1/f$ noise due to its significance in deep submicron CMOS devices. Our investigation showed that using a SiGe channel generally improves the device’s DC and RF characteristics. Our evidence
proves that this device is particularly advantageous in suppressing the 1/f noise, even after gate-oxide degradation by electrical stress.

II. Device Fabrication and Measurements

We used reduced-pressure chemical vapor deposition to grow Si/Si_{0.8}Ge_{0.2}/Si quantum well structures on lightly doped n-type silicon substrates. The epitaxy started with a Si seed that was 10 nm thick, and a growth of a 20 nm thick Si_{0.8}Ge_{0.2} channel followed it. Subsequently, a Si-cap layer with a thickness of 6 nm was deposited on the substrate. All epilayers were grown at 600 °C–700 °C without intentional doping. After isolating the device, we grew the gate oxide in an H_{2}/O_{2} ambient (H_{2}:O_{2}=1:2) at 800 °C. We processed the samples, including a Si-control, to produce pMOSFETs with a gate length of 0.5 µm. The gate oxide thickness was approximately 7 nm for both the Si_{0.8}Ge_{0.2} and all-Si samples. Figure 1 shows the schematic cross-sectional view of the Si_{0.8}Ge_{0.2} pMOSFET with an energy band diagram. The average thickness of the unconsumed Si-cap layer in the Si_{0.8}Ge_{0.2} sample was 2 nm, measured by transmission electron microscopy.

The samples were characterized by an on-wafer test using an HP4156B semiconductor parameter analyzer for dc measurement and an HP8510C network analyzer for cutoff frequency \( f_{T} \), maximum oscillation frequency \( f_{max} \), and minimum noise figure \( NF_{min} \) measurements. The 1/f noise was measured by a setup consisting of an Agilent E4440A spectrum analyzer with an EG&G 5185 wideband low noise preamplifier for 10 Hz–1 MHz. The normalized drain current spectral density \( S_{n}/I_{d} \) was derived from the fluctuation in drain voltage \( V_{ds} \). The number of averages used in the 1/f noise measurement was 50. All measurements were performed at room temperature.

III. Results and Discussion

1. DC Characteristics

Figures 2(a) and 2(b) illustrate the transfer and output characteristics of the Si_{0.8}Ge_{0.2} and all-Si pMOSFETs, respectively. The Si_{0.8}Ge_{0.2} sample exhibited higher drain current \( I_{d} \) and extrinsic transconductance \( g_{m} \) for the same gate overdrives. Since both samples showed minor differences in source/drain series \( R_{sd} = 1.9 ± 0.1 \) Ω mm and contact \( R_{c} = 8 ± 1 \) Ω/sq., we attributed the improvement in performance mainly to the better carrier transport in the Si_{0.8}Ge_{0.2} channel at this gate length. As Table 1 shows, the Si_{0.8}Ge_{0.2} sample revealed 63% and 12% larger \( g_{m} \) values in the linear \( V_{ds} = –0.1 \) V, \( V_{gs} = V_{th} – 0.7 \) V and saturation \( V_{ds} = –3 \) V, \( V_{gs} = V_{th} – 0.7 \) V) regions, respectively. The intrinsic transconductance \( g_{m-intra} \) values inserted in the table also showed similar behavior. Correspondingly, \( I_{d} \) was enhanced by 16% in the linear and 14% in the saturation region at the given bias. This indicated that a high-mobility Si_{0.8}Ge_{0.2} buried channel had effectively formed in the device, and this had improved the device’s driving ability.

To estimate the hole distribution in the Si and Si_{0.8}Ge_{0.2} pMOSFETs, we performed a two-dimensional device simulation using SILVACO. Figure 3 illustrates the result. The buried channel in the Si_{0.8}Ge_{0.2} device was formed at the Si-cap/Si_{0.8}Ge_{0.2} interface; this means that the oxide-to-channel distance was purely determined by the unconsumed Si-cap thickness. The ratio of the hole density in the Si-cap to the total hole density \( N_{Si-cap}/(N_{Si-cap}+N_{SiGe}) \) was 19.7\% at \( V_{gs} = V_{th} – 0.7 \) V. However, the parasitic conduction in the Si_{0.8}Ge_{0.2} device was minimal because carriers located closer to the oxide interface have much lower mobilities [9]. Consequently, we considered that the conduction in the Si_{0.8}Ge_{0.2} pMOSFET was dominated by the Si_{0.8}Ge_{0.2} buried channel.

Table 1 compares other DC parameters of the samples, such as off-current \( I_{off} \), \( V_{th} \) subthreshold swing \( S \), and drain-induced barrier lowering (DIBL). The Si_{0.8}Ge_{0.2} sample showed a more positive \( V_{th} \) of \(-0.961 \) V than that of the all-Si sample \(-1.141 \) V. In fact, we expected a lower \( V_{th} \) in the Si_{0.8}Ge_{0.2} pMOSFET because the holes are mainly located in the Si-cap/Si_{0.8}Ge_{0.2} interface; this leads to a quicker turn-on of the buried channel than the surface one [5]. Meanwhile, the Si and Si_{0.8}Ge_{0.2} pMOSFETs revealed similar \( I_{off} \) and \( S \) values in the range of \( 4.7×10^{-10} \) µA/µm–\( 5.4×10^{-10} \) µA/µm and 79.3 mV/dec–80.2 mV/dec, respectively, whereas
there was a slight improvement in DIBL in the Si$_{0.8}$Ge$_{0.2}$ sample. (The DIBL was extracted from a $V_{th}$ shift in the log $|I_d|$ – $V_{ds}$ curves between $V_{th} = -0.1$ V and $-3.0$ V.) The carrier confinement in the Si$_{0.8}$Ge$_{0.2}$ buried channel seemed to lead to a lower gate-controlled depletion charge and electric field (i.e., smaller band bending) in the subsurface [10]. These in

Table 1. DC parameters of the Si$_{0.8}$Ge$_{0.2}$ and Si pMOSFETs.

<table>
<thead>
<tr>
<th>DC parameters</th>
<th>Si$<em>{0.8}$Ge$</em>{0.2}$</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>I_d</td>
<td>$ (mA/µm)</td>
</tr>
<tr>
<td>saturation ($V_{ds} = -3$ V)</td>
<td>$1.51 \times 10^{-2}$</td>
<td>$1.32 \times 10^{-2}$</td>
</tr>
<tr>
<td>$g_m$ (mS/µm)</td>
<td>linear ($V_{ds} = -0.1$ V)</td>
<td>$6.26$</td>
</tr>
<tr>
<td>saturation ($V_{ds} = -3$ V)</td>
<td>$42.5$ (47.3)</td>
<td>$37.9$ (42.6)</td>
</tr>
<tr>
<td>$</td>
<td>I_{off}</td>
<td>$ (mA/µm)</td>
</tr>
<tr>
<td>$V_{th}$ (V)</td>
<td>$-0.961$</td>
<td>$-1.141$</td>
</tr>
<tr>
<td>$S$ (mV/dec)</td>
<td>$80.23$</td>
<td>$79.29$</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>$8.68$</td>
<td>$12.36$</td>
</tr>
</tbody>
</table>

turn suppressed hole flowing from the source to the drain in the subthreshold region, and then finally improved the DIBL. We concluded that the Si$_{0.8}$Ge$_{0.2}$ channel did not degrade the device’s turn-off characteristic and short channel immunity.

2. $f_T$/$f_{max}$ and $NF_{min}$ Characteristics

Figure 4 illustrates $f_T$ and $f_{max}$ versus $|V_{gs} - V_{th}|$ of the Si and Si$_{0.8}$Ge$_{0.2}$ pMOSFETs. As expected, the Si$_{0.8}$Ge$_{0.2}$ pMOSFET showed increased $f_T$ and $f_{max}$ values, owing to the improved carrier transport in the Si$_{0.8}$Ge$_{0.2}$ channel.

For instance, the maximum $f_T$ and $f_{max}$ occurred at a $|V_{gs} - V_{th}|$
of 2.0 V–2.5 V for both samples, when \( V_{ds} \) was fixed at –3 V. At the given bias, the Si_{0.8}Ge_{0.2} pMOSFET experienced approximately 20% improvements in both \( f_{T} \) and \( f_{max} \). However, the benefits of the Si_{0.8}Ge_{0.2} channel diminished as \( |V_{gs}–V_{th}| \) increased up to 3.5 V. This is because the carrier transport in the device tends to be dominated by the low-mobility parasitic surface channel at a large gate overdrive [11].

\[ f_{T}, f_{max} (GHz) \]

\[ V_{ds} = -3 V \]

\[ L/W = 0.5 \mu m/30 \mu m \]

Figure 4. \( f_{T}, f_{max} \) vs. \( |V_{gs}–V_{th}| \) of the Si_{0.8}Ge_{0.2} and Si pMOSFETs at the given bias.

Figure 5 shows the \( NF_{min} \) versus the frequency plots of the Si and Si_{0.8}Ge_{0.2} pMOSFETs at the given bias. Unlike in \( f_{T}/f_{max} \) cases, de-embedding was not performed in the \( NF_{min} \) measurement. The Si_{0.8}Ge_{0.2} sample exhibited generally lower \( NF_{min} \) levels in the given frequency range. \( NF_{min} \) is a function of \( g_{m} \) as represented in (1),

\[ NF_{min} = 1 + K \frac{2\pi C_{g} f}{g_{m}} \sqrt{R_{g} + R_{i} + R_{s}} \]

where \( K \) is the stability factor; \( C_{g} \) is the gate capacitance; \( R_{g}, R_{i}, \) and \( R_{s} \) are gate resistance, input resistance, and source resistance, respectively. Because \( NF_{min} \) is a function of \( g_{m} \), we speculated that the lower \( NF_{min} \) levels of the Si_{0.8}Ge_{0.2} pMOSFET were from its larger \( g_{m} \) values.

3. 1/f Noise Characteristics

Figure 6 shows \( S_{f}/L_{f}^2 \) versus the frequency of the Si and Si_{0.8}Ge_{0.2} pMOSFETs at the given bias. Clearly, the Si_{0.8}Ge_{0.2} sample shows much lower 1/f noise levels, by a factor of around \( 10^{2} \), than the Si-control. The dependence of \( (WL) \times S_{f}/L_{f}^2 \) at 30 Hz on \( |V_{gs}–V_{th}| \) for both samples is illustrated in Fig. 7. The noise values of SiGe pMOSFETs from references [5] and [11] were also included for comparison. The improvement in 1/f noise reduced as the gate overdrive increased. As previously mentioned, this was probably due to the enhanced parasitic conduction in the Si_{0.8}Ge_{0.2} sample at a large gate bias. The lower 1/f noise in SiGe pMOSFETs has been conventionally explained by a reduction in carrier number fluctuation (\( \Delta n \)) involving trapping/detrapping of holes near the oxide interface. The suppressed charge exchange between oxide traps and the buried channel are responsible for it. In addition,
Mathew et al. suggested that the oxide trap density \( N_{ox} \) close to the Fermi level \( (E_F) \) is much lower in SiGe pMOSFETs [12]. They attributed this to the larger displacement of the hole quasi-Fermi level from the valence band edge at the oxide interface \( (E_{v_{ox}}) \) for the same gate overdrive [13]. The reduced 1/f noise in the Si\(_{0.8}\)Ge\(_{0.2}\) pMOSFET also indicates the high quality of the epilayers and gate-oxide (interface) in the sample.

![Graph](image)

**Fig. 7.** Dependence of \( (WL) \times S_{I_d}^2 \) at 30Hz on \( |V_{gs}-V_{th}| \) for the Si\(_{0.8}\)Ge\(_{0.2}\) and Si pMOSFETs. The noise data from [5] and [11] are also included for comparison.

To investigate the relationship between the gate oxide condition and 1/f noise, we measured the 1/f noise of both samples again after applying a constant \( V_{gs} \) of \(-8\) V for 120 seconds with the drain and source contacts grounded. Table 2 shows the variations in \( V_{th} \) and hole mobility after electrical stress. The hole mobility was obtained from the \( g_m \) measurement at \( V_{ds} = -0.1 \) V, \( V_{gs} = V_{th} - 0.7 \) V. Figure 8 also graphically compares the variations in 1/f noise due to stress.

![Graph](image)

**Fig. 8.** Variations in \( S_{I_d}^2 \) after the electrical stress for the Si\(_{0.8}\)Ge\(_{0.2}\) and Si pMOSFETs.

We attributed the observed \( V_{th} \) shift towards negative values to the trapped charges (holes) near the oxide, and both samples showed degradations in mobility (or \( g_m \)) and 1/f noise after stress. The elevation of the noise level after the stress confirmed that the creation of traps near the oxide was responsible for noise generation, along with mobility reduction and the \( V_{th} \) shift. It is clear that the 1/f noise levels of both samples almost uniformly shifted upwards after stress, as revealed in the log-scale plot. This agrees with the presumption that the buried channel device is less noisy than the surface channel device, regardless of gate oxide degradation by electrical stress. The almost identical relative changes in the noise reflected the identical relative changes in \( N_{ox} \) at \( E_F \), even though the initial \( S_{I_d}^2 \) and \( N_{ox} \) values of the samples covered a wide range.

\[
N_{ox} = \frac{WLC_{gc}^2 f S_{I_d}}{q^{2} kT \lambda},
\]

where \( W \) and \( L \) are the gate width and gate length, respectively, \( C_{gc} \) is the gate-to-channel capacitance per unit area, and \( f \) is the frequency. \( S_{I_d} \), which is the input referred noise spectral density in the linear region, is obtained by

\[
S_{I_d} = \frac{S_{I_d}}{I_d^2 \left( g_m \right)}.
\]

where \( q \), \( k \), \( T \) and \( \lambda \) are respectively the electron charge,
Boltzmann’s constant, temperature, and McWhorter’s tunneling parameter (typically 1 Å). The $N_{ox}$ calculations of the Si-control are $5.2 \times 10^{17} \text{cm}^{-2}\text{eV}^{-1}$ and $1.2 \times 10^{18} \text{cm}^{-2}\text{eV}^{-1}$ (i.e. $\Delta N_{ox}/N_{ox} = 131\%$) at 30 Hz before and after stress, respectively. Since (2) is only valid for a standard surface channel MOSFET, it is difficult to apply the equation directly to a SiGe pMOSFET due to the existence of a parasitic surface channel in it [14]. However, the equation may be effectively used for the SiGe pMOSFET with minimal parasitic conduction, assuming that $\lambda$ is equal to that used for the standard Si MOSFET [13], [14]. We reasonably applied the equation to the Si$_{0.8}$Ge$_{0.2}$ pMOSFET in this study and found that the $N_{ox}$ calculations at 30 Hz varied from $7.9 \times 10^{15} \text{cm}^{-2}\text{eV}^{-1}$ to $1.4 \times 10^{16} \text{cm}^{-2}\text{eV}^{-1}$ ($\Delta N_{ox}/N_{ox} = 77\%$) after stress. The variations in $N_{ox}$ might be regarded as a uniform shift, as in the previous $S_{1}/I_{d}$ case, although a slightly larger percentage change in $N_{ox}$ is observed in the Si-control. Thus, we concluded that the tunneling electrons created the oxide traps during stress at a rate proportional to their initial number for the Si and Si$_{0.8}$Ge$_{0.2}$ pMOSFETs.

IV. Conclusions

We investigated the DC and RF characteristics of a Si$_{0.8}$Ge$_{0.2}$ pMOSFET. The Si$_{0.8}$Ge$_{0.2}$ device revealed larger $g_{m}$, $|I_{d}|$, $f_{T}$, and $f_{max}$ levels, which we considered were responsible for the improved carrier transport in the Si$_{0.8}$Ge$_{0.2}$ channel, while maintaining $I_{off}$ and $S$ values. Particularly, our results demonstrated that the 1/f noise in the Si$_{0.8}$Ge$_{0.2}$ pMOSFET was much lower, by a factor of $10^{5}$, than in the all-Si sample, before and after electrical stress. Meanwhile, both samples showed almost identical relative changes in 1/f noise after the oxide degradation by electrical stress. Our results confirm that the Si$_{0.8}$Ge$_{0.2}$ pMOSFET has enhanced operation speed and lower 1/f noise compared to the standard Si pMOSFET.

References


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