The design and performance of an InGaAs/InP transimpedance amplifier and post amplifier for 40 Gb/s receiver applications are presented. We fabricated the 40 Gb/s transimpedance amplifier and post amplifier using InGaAs/InP heterojunction bipolar transistor (HBT) technology. The developed InGaAs/InP HBTs show a cut-off frequency ($f_T$) of 129 GHz and a maximum oscillation frequency ($f_{max}$) of 175 GHz. The developed transimpedance amplifier provides a bandwidth of 33.5 GHz and a gain of 40.1 dB. A 40 Gb/s data clean eye with 146 mV amplitude of the transimpedance amplifier module is achieved. The fabricated post amplifier demonstrates a very wide bandwidth of 36 GHz and a gain of 20.2 dB. The post-amplifier module was fabricated using a Teflon PCB substrate and shows a good eye opening and an output voltage swing above 520 mV.

Keywords: InGaAs/InP HBT, 40 Gb/s, transimpedance amplifier, post amplifier, module, package.
Fig. 1. Typical DC and RF characteristics of an InGaAs/InP HBT with an emitter area of 6 µm².
overall bandwidth transimpedance amplifier. In this work, we carried out a circuit simulation including loss by transmission lines in the circuit. When we considered the line effect, the transimpedance gain of the transimpedance amplifier was reduced as the frequency was increased. The effective transimpedance gain without a photo detector was measured on-wafer using coplanar probes.

The transimpedance amplifier exhibited an $S_{21}$ gain of 9.9 dB, and $S_{22}$ was less than –5 dB over a frequency range of less than 40 GHz. The transimpedance gain ripple was about 3.7 dB, and measured group delay was about 44 ps. The power dissipation was 82.5 mW with a single voltage supply of 3.3 V. These characteristics make the transimpedance amplifier suitable for use in a high-speed optical receiver.

For packaging processes, the whole wafer was sliced into separate chips. Each chip was mounted on a patterned ceramic substrate and wire bonded and assembled in an Au-plated metal case with SMA connectors for input and output ports. Figure 4(a) shows the assembled transimpedance amplifier module and Fig. 4(b) shows the small signal response of the packaging components, including the ceramic substrate, housing, connector, and wire-bonding. A low electrical return loss over a wide frequency range and an insertion loss of 1.5 dB at 40 GHz were achieved. To reduce the parasitic loss, the ceramic substrate had a hole and slot. By mounting the transimpedance amplifier in the hole, the wire length was minimized, and by adopting a substrate slot structure, the in-out coupling was suppressed. We fabricated transimpedance amplifier modules as shown in Fig. 5(a). To measure the eye-diagram, we made a 40 Gb/s NRZ signal by multiplexing 4-channel 10 Gb/s PPG signals (pseudorandom binary sequence $2^31−1$). As shown in Fig. 5(b), the 40 Gb/s NRZ eye diagrams of the finally packaged transimpedance amplifier show a clear eye with a pattern of 146 mV for an input of 50 mV with rise and fall times of less than 10 ps.
IV. Characteristics of Post-Amplifier Module

The post amplifier had a two-stage differential design. The two differential stages were coupled with emitter followers to transform the impedance and to shift the DC level. A differential operation was applied to reduce the time jitter and crosstalk. The overall chip layout was designed to keep the symmetry between differential signals to reduce the offset.

The chip size, including electrode pads for on-wafer measurement and the packaging wire bond, was 1.0 mm × 0.9 mm. Figure 6 shows a photograph of the post amplifier. RF signal pads for the differential input and output were configured into a signal-ground-signal type with a 150 µm pitch on both the left and right sides. Large ground and power supply areas were used to obtain a low impedance and large capacitance. The circuit is composed of an input buffer, a two-stage amplifier, and an output buffer. The output buffer supplies constant differential voltages above 500 mV through a 50 ohm output resistor.

Figure 7 shows the gain bandwidth characteristics for the post amplifier. The fabricated amplifier exhibited a 36 GHz bandwidth with a single-ended 20.2 dB small-signal gain and an overall differential gain above 25 dB when the bias voltage was –4.9 V.

For packaging processes, the entire wafers were lapped, Au was evaporated onto the back side, and the wafers were sliced into separate chips. The chips were mounted onto a patterned board, wire bonded, and assembled in an Au-plated metal case with V-connectors. We adopted a Teflon PCB substrate for low cost application. The Teflon PCB substrate was 5 mils thick and was patterned using 0.5 ounce copper.

The GSG coplanar line between the post amplifier pad and V-connector was a patterned coplanar waveguide transmission line with 50 ohm characteristic impedance. Ground vias of
3 mm in diameter were designed to connect the top grounds to the back metallization. We used 100 pF single-layer capacitors and 10 nF multi-layer capacitors to bypass RF signals in the DC bias line. Figure 8 shows the assembled post-amplifier module.

Figure 9 shows the eye patterns for a post-amplifier module measured using a single-ended input voltage swing of 160 mV and a 50 mV input signal. As seen in Fig. 9, the 40 Gb/s NRZ eye diagrams of the finally packaged post amplifier show open 40 Gb/s eyes with an output magnitude above 520 mV with rise and fall times of less than 10 ps.

We conducted temperature and humidity tests of the post-amplifier module. Figure 10 shows the temperature and humidity test cycle. As seen in Table 1, there is no remarkable gain variation or abnormal current flooding during the test cycle, which confirms the reliability of the fabricated post-amplifier module.

V. Conclusion

In conclusion, we have successfully developed a wideband transimpedance amplifier and post amplifier using InGaAs/InP HBT technology. InGaAs/InP technology is preferred for the design and fabrication of 40 Gb/s electrical components. Experimental results demonstrate a transimpedance of 40.1 dB and 33.5 GHz bandwidth with S-parameters measured. The power consumption of the amplifier is 82.5 mW and the chip size is 0.354 mm². Transimpedance amplifier modules were fabricated using ceramic substrates and wire bonding. We applied the hole and slot structure to the substrate design to reduce parasitic loss and coupling. Eye diagram measurements for transimpedance amplifier modules were carried out at a data rate of 40 Gb/s. Clear open eye diagrams at 40 Gb/s data rates were achieved.

A post amplifier was also fabricated using InGaAs/InP HBT technology. The fabricated circuit had an S21 gain of 20.2 dB and a –3 dB bandwidth of 36 GHz, with an excellent eye opening for a 40 Gb/s random pattern signal. Clear 40 Gb/s eye diagrams demonstrated the good system applicability of this module. The broadband transimpedance amplifier module and post-amplifier module are adequate for 40 Gb/s optical transport network systems.

References

communications systems. MMIC design for wireless telecommunications and optical research interests include compound semiconductor devices and development of InGaP/GaAs devices and power amplifier circuits. His optical fiber communication. Recently, he has been engaged in on high-frequency heterojunction devices and ICs for long distance Telecommunications Research Institute (ETRI), where he has worked optical communications systems since 1998.

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