This paper presents a clock and data recovery circuit that supports dual data rates of 5.4 Gbps and 3.24 Gbps for DisplayPort v1.2 sink device. A quarter-rate linear phase detector (PD) is used in order to mitigate high speed circuit design effort. The proposed linear PD results in better jitter performance by increasing up and down pulse widths of the PD and removes dead-zone problem of charge pump circuit. A voltage-controlled oscillator is designed with a 'Mode' switching control for frequency selection. The measured RMS jitter of recovered clock signal is 2.92 ps, and the peak-to-peak jitter is 24.89 ps under 2^{31}–1 bit-long pseudo-random bit sequence at the bitrate of 5.4 Gbps. The chip area is 1.0 mm×1.3 mm, and the power consumption is 117 mW from a 1.8 V supply using 0.18 µm CMOS process.

Keywords: Linear phase detector, clock and data recovery, quarter-rate PD, dual-rate voltage controlled oscillator (VCO), DisplayPort.
quarter-rate PD generating enlarged up/down pulse widths and charge pump (CP) blocks are proposed.

The dual-loop architecture consists of a frequency-acquisition loop and a phase-locked loop [2], [3], [6], [8]. During the frequency locking process (Loop 1), the frequency detector (FD) compares the frequency difference between an external reference clock and recovered clock. When the rising edge of the REF_CLK stays within two adjacent phase clocks for a certain period, the frequency lock detector sends the lock signal to shift the operation from the frequency acquisition process to the phase locking process. During the phase locking (Loop 2), the clock is recovered and the data are retimed. Since the first draft version of DisplayPort v1.2 standard should support the dual data rates (3.24 Gbps and 5.4 Gbps), the dual-rate voltage-controlled oscillator (VCO) is designed. The target clock frequency can be selected by the ‘Mode’ signal generated by the DisplayPort link layer detecting the input data rate. At ‘Mode 0’, the VCO operates at 810 MHz, which is a quarter rate of 3.24 Gbps input data. At ‘Mode 1’, the VCO generates a 1.35 GHz clock for 5.4 Gbps data. The DisplayPort leaves the designer as an option for the CDR design whether using a reference clock or not using a reference clock (reference-less CDR). In this paper, the CDR with reference clock is adopted for the faster lock.

III. Building Block Design

1. Enhanced Quarter-Rate Linear PD

Figure 2 shows the proposed quarter-rate linear PD. The proposed PD consists of latches, XOR, and AND gates. The two outputs from the second (CLK90') and first (CLK90) latches are compared by XOR gates and generate UP[3:0] signals. These UP[3:0] signals also make DN[3:0] signals through the AND gates’ operation with the four phase-recovered clocks from VCO (CLK0", CLK90", CLK180" and CLK270"). Also, the A, B, C, and D outputs are provided to the data recovery (DR) block to retime the data. Linear PD is affected by clock duty and unwanted gate delay mismatch due to parasitic elements. In practice, the proposed PD is implemented with clock and data buffer for delay matching. In this work, all gates in the PD are implemented with current mode logic for supporting high-speed operation.

In the quarter-rate PD operation, the up pulse width is proportional to the phase error, whereas the down pulse width is constant regardless of the phase error. In the locked state, the up pulse width is 2.5 times of 1-bit data period (2.5×TBIT) and down pulse width is twice of data rate (2.0×TBIT). Thus, the ratio of the up and down pulse widths is 5/4. The difference between up and down pulse widths can be compensated by the CP with a reverse current ratio.

The timing diagram of the quarter-rate linear PD is shown in Fig. 3. Waveforms, A, B, C, and D are the first latch outputs and E, F, G, and H are the second latch outputs. Figure 4 shows the comparison of the simulated current mismatch effect in the...
Fig. 3. Timing diagram of proposed quarter-rate linear PD.

Fig. 4. Simulated current mismatch effect by up/down pulse width: (a) reference PD (1.5×T_BIT) and (b) proposed PD (2.5×T_BIT). Mismatch ratio: A/B.

Table 1. Comparison of proposed quarter-rate linear PD with other subrate linear PDs (T_BIT = width of one bit data).

<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of PD</td>
<td></td>
<td>Quarter-rate</td>
<td>Quarter-rate</td>
<td>Half-rate</td>
<td>Full-rate</td>
</tr>
<tr>
<td>Pulse width</td>
<td>Up</td>
<td>2.5×T_BIT</td>
<td>3.5×T_BIT</td>
<td>1.5×T_BIT</td>
<td>0.5×T_BIT</td>
</tr>
<tr>
<td></td>
<td>Down</td>
<td>2.0×T_BIT</td>
<td>4.0×T_BIT</td>
<td>1.0×T_BIT</td>
<td>0.5×T_BIT</td>
</tr>
</tbody>
</table>

Figure 5 shows the simulated PD gain for each data rate. The pulse widths of a generated up/down pulses (PD output) versus phase difference between the data edge and clock edge are plotted for each data rate.

Table 1 shows the comparison of the proposed quarter-rate linear PD with other subrate linear PDs published before. When the PD in [3] is compared with the PD in [4], the difference is an increased up pulse width. Compared to the PDs in [3]-[5], the proposed PD has the longer pulse width. Comparing the proposed PD to [2], the proposed PD’s pulse widths are equivalent to 4×T_BIT (up pulse) and 5×T_BIT (down pulse), respectively, if it is modified to 1/8 rate PD as in [2]. As a result, the proposed PD has the widest pulse width. Hence, it can show the better jitter performance. Though the pulse width is increased, total current consumption can be controlled by adjusting the CP current.

2. VCO with Mode Control

Since the CDR should support two different data rates, the VCO should generate two different frequencies. At each frequency, the VCO generates four different phase clocks for the quarter-rate PD. The ring oscillator type VCO is proposed with a digital mode switch for selecting the operating frequency. The frequency ‘Mode’ value is provided from the link layer.
Figure 6 shows the schematic of the proposed dual-rate VCO delay cell. The load of the differential pair is made up of p-channel metal-oxide-semiconductor field-effect transistor (PMOS). According to (1), the delay of the delay cell can be decided by the load effective resistance and capacitance:

\[ t_d = R_{\text{eff,load}} \times C_{\text{eff, out}} \]  

(1)

The VCO changes its effective resistance by adding PMOS (M9-M10) elements which are controlled by the ‘Mode’ signal. At ‘Mode 0’, the M9 and M10 are in the cut-off (switch-off) region and the node is in open state. At ‘Mode 1’, the M9 and M10 are in the linear region (switch-on) and they act like an additional resistor. Assuming that the total effective resistance at ‘Mode 0’ is \( R_{\text{eff,0}} \) and the effective resistance of M9 and M10 is \( R_{\text{m9,10}} \), the total effective resistance at ‘Mode 1’ will be \( R_{\text{eff,1}} || R_{\text{m9,10}} \) and it is smaller than \( R_{\text{eff,0}} \). Consequently, according to (2), the time delay at ‘Mode 1’ is shorter than at ‘Mode 0’. Thus, two target frequencies (810 MHz and 1.35 GHz) are controlled by the ‘Mode’ signal.

\[ R_{\text{eff,0}} \geq R_{\text{eff,1}} || R_{\text{m9,10}} \]  

(2)

The proposed VCO also adds current source to decrease VCO gain, and it covers all tuning range of the VCO. Simulations show that the gains of VCO are 920.55 MHz/V at 3.24 Gbps and 832.48 MHz/V at 5.4 Gbps, as shown in Fig. 7(a). Corner simulations show that the target frequency ranges are safely covered under the process, supply voltage, and temperature (PVT) variations. The simulated VCO phase noise shows –80 dBc/Hz and –88 dBc/Hz at 1 MHz offset from 810 MHz and 1.35 GHz clock frequency, respectively, as shown in Fig. 7(b).

3. CP Circuit

The CP circuit is shown in Fig. 8. A unity gain buffer is used to clamp the terminal voltages of current sources during the zero-current pumping period. In this way, glitches on the loop filter due to the charge sharing can be minimized. Since the up and down pulse widths of the PD are different, two different bias current sources are placed. The up/down current ratio is set to be 4/5 (reverse of the up/down pulse width ratio). The up and down current values of the CP are 12 \( \mu \)A and 15 \( \mu \)A, respectively, in the CDR loop. If the CP has a \( \pm 5\% \) current mismatch due to PVT variations, 0.08 UI of data eye is affected.

4. Data Recovery

Since the proposed CDR recovers the data with the quarter-
5. Frequency Lock Detector

Figure 11 shows the frequency lock detector block. The resolution of the frequency lock detector is determined by (3). Thus, the frequency detection resolution can be improved by increasing the number of the counter bit size. The timing diagram of the frequency lock detector is shown in Fig. 12. If the reference clock is located between zero phase clock (CLK0) and 90 degree phase clock (CLK90) for a certain period, the frequency lock signal is on. After the frequency lock detector generates the lock signal, the lock signal makes the CDR shift the operation from the frequency acquisition process to the phase locking process. Since the 4-bit counter is used in this design, the lock signal is on if the generated clocks (CLK0, CLK90) stay at the same position during continuous 16 reference clock period.

\[
\delta = \frac{90^\circ}{2^{\text{bit_counter}}} = \pm1.56\%.
\]  

IV. Measurement Results

The CDR circuit using the quarter-rate linear PD with enhancing the CP pulse width has been fabricated in a 0.18-μm complementary metal-oxide-semiconductor (CMOS) RF technology. The chip consumes 117 mW at 5.4-Gbps data rate. The chip microphotograph is shown in Fig. 13. Loop bandwidth of the implemented CDR has 10 MHz, and its capacitances were implemented using metal-insulator-metal capacitor for accurate capacitance on the chip. Also, the loop
Fig. 13. Photomicrograph of proposed chip.

Fig. 14. Jitter measurement result: recovered data eye and jitter histogram of recovered clock (a) at 5.4 Gbps PRBS input data and (b) at 3.24 Gbps PRBS input data.

The core area of the CDR circuit is 1 mm×1.3 mm. For facilitating the measurements, a test chip was mounted on a FR-4 printed circuit board using bonding wires.

Figure 14 shows the measured eye-diagram of the recovered half-rate data output and recovered clock for 231–1 pseudo-random bit sequence (PRBS) input data at 5.4 Gbps and 3.24 Gbps. The measured RMS jitter and peak-to-peak jitter of the recovered clock are 2.92 ps and 24.89 ps at 5.4 Gbps, and 4.55 ps and 27.4 ps at 3.24 Gbps, respectively. The bit error rate is measured to be less than 10⁻¹² at both data rates with PRBS 2³¹–1 data format. Figure 15 illustrates the jitter tolerance at 5.4 Gbps. It shows that the designed circuit meets the jitter tolerance specification.

The performance comparison of the proposed CDR is given in Table 2. The proposed one and previous 5-Gbps CDRs with the same process were compared. The proposed circuit shows better jitter and power consumption performance. Since [3] and [4] adopted LC-VCO rather than ring oscillator type VCO and designed for a 10 Gbps data rate, the measurement data of [3] and [4] were not included in the comparison table.

Table 2. Performance summary of proposed CDR and other works.

<table>
<thead>
<tr>
<th>Specification</th>
<th>This work</th>
<th>[2]</th>
<th>[5]</th>
<th>[9]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (CMOS)</td>
<td>0.18 µm</td>
<td>0.18 µm</td>
<td>0.18 µm</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Data rate</td>
<td>3.24/5.4 Gbps</td>
<td>5 Gbps</td>
<td>5 Gbps</td>
<td>155 Mbps to 3.125 Gbps</td>
</tr>
<tr>
<td>PD type</td>
<td>Quarter-rate</td>
<td>1/8-rate</td>
<td>Full-rate</td>
<td>Full-rate</td>
</tr>
<tr>
<td>Clock jitter (RMS) (@2³¹–1 PRBS)</td>
<td>2.92 ps (@5.4 Gbps)</td>
<td>4.55 ps (@3.24 Gbps)</td>
<td>6.8 ps (@5 Gbps)</td>
<td>6.04 ps (@5 Gbps)</td>
</tr>
<tr>
<td>Power consumption (w/o I/O buffer)</td>
<td>117 mW (@5.4 Gbps)</td>
<td>144 mW</td>
<td>130 mW</td>
<td>95 mW</td>
</tr>
</tbody>
</table>

V. Conclusion

A CDR circuit that supports dual data rates of 5.4 Gbps and 3.24 Gbps for DisplayPort v1.2 sink device is presented in this paper. The CDR is realized with a quarter-rate PD with enhancing the up and down pulses. The proposed CDR circuit is fabricated in a 0.18-µm CMOS technology, and it shows 2.92-ps RMS and 24.89-ps peak-to-peak jitter in the recovered quarter-rate clock from 2³¹–1 PRBS at 5.4-Gbps serial input.

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References


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