In this paper, MOS-triggered silicon-controlled rectifier (SCR)-based electrostatic discharge (ESD) protection circuits for mobile application in 3.3 V I/O and SCR-based ESD protection circuits with floating N+/P+ diffusion regions for inverter and light-emitting diode driver applications in 20 V power clamps were designed. The breakdown voltage is induced by a grounded-gate NMOS (ggNMOS) in the MOS-triggered SCR-based ESD protection circuit for 3.3 V I/O. This lowers the breakdown voltage of the SCR by providing a trigger current to the P-well of the SCR. However, the operation resistance is increased compared to SCR, because additional diffusion regions increase the overall resistance of the protection circuit. To overcome this problem, the number of ggNMOS fingers was increased. The ESD protection circuit for the power clamp application at 20 V had a breakdown voltage of 23 V; the product of a high holding voltage by the N+/P+ floating diffusion region. The trigger voltage was improved by the partial insertion of a P-body to narrow the gap between the trigger and holding voltages. The ESD protection circuits for low- and high-voltage applications were designed using 0.18 µm Bipolar-CMOS-DMOS technology, with 100 µm width. Electrical characteristics and robustness are analyzed by a transmission line pulse measurement and an ESD pulse generator (ESS-6008).

Keywords: ESD protection circuit, ggNMOS, SCR, trigger voltage, holding voltage.

I. Introduction

The demand for low- and high-voltage technologies for analog and smart power integrated circuit (IC) applications is growing these days. Consequently, low- and high-voltage ICs are widely used in power management, display drivers, and automotives [1]–[3]. The reliability to withstand an electrostatic discharge (ESD) is regarded as an important issue for low- and high-voltage products. With the development of processing technology, the ESD phenomenon has emerged as a key issue in relation to the reliability of ICs. Although the development of processing brought about the miniaturization of ICs, malfunction and breakdown in the normal state due to the ESD phenomenon have increasingly been recognized as a serious problem [4]. In general, to prevent the ESD phenomenon from damaging semiconductor devices, while it is also important to improve the manufacturing environment or transportation conditions of the ICs, it is essential to add an ESD protection circuit into the manufacture of semiconductor chips. Because the ESD phenomenon occurs randomly at any of the external input/output terminals, an ESD protection circuit must be installed at every external input/output terminal. ESD protection circuits must not affect the normal operation of the internal circuit and must maintain the turn-off state. For this purpose, they must be designed in such a manner that they will work in a region called the ESD design window [5].

In smart power IC technology, grounded-gate NMOS (ggNMOS) and silicon-controlled rectifier (SCR) are generally used as ESD protection circuits. A ggNMOS is easy to design and perfectly compatible with CMOS technology. However, a ggNMOS is not appropriate for power clamp terminals that require the characteristics of high robustness, as it is vulnerable to degradation near a low oxide film due to its high surface...
current density, and it has a very small amount of ESD current per area that can be discharged (only a few mA/µm). The SCR-based ESD protection circuit is appropriate for high-voltage ESD protection, due to its respectable current driving ability and excellent ESD robustness characteristics per area, because it forms a current path inside a silicon substrate [6]. However, it is not appropriate for low- and high-voltage protection circuits due to the high trigger voltage caused by an avalanche breakdown between the N-well and P-well, and low holding voltage, which is the turn-on voltage of the NPN/PNP bipolar. As a result, to use an SCR as an ESD protection circuit in a low-voltage IC, the problems of high trigger voltage and low holding voltage must be solved. First, it is difficult to apply an SCR to mobile application circuits using a 3.3 V I/O, because the high trigger voltage causes a breakdown of the internal circuit. Second, the low holding voltage causes latch-up by overshoot voltage and noise. Therefore, an efficient ESD protection circuit with a low trigger voltage and high holding voltage is required [7]. Furthermore, due to the aforementioned problems, it is impossible to apply an SCR-based protection circuit to ICs for a 20 V power clamp.

In this paper, the structure of an SCR was changed to design an ESD protection circuit corresponding to the ESD design window of mobile devices, notebooks, and light-emitting diode (LED) driver applications that use 3.3 V I/O and 20 V power clamps. The 3.3 V/20 V ESD protection circuit was designed through a 0.18 µm Bipolar-CMOS-DMOS (BCD) technology at a 100 µm width, and its electrical characteristics and robustness were verified through a transmission line pulse (TLP) measurement and an ESD pulse generator (ESS-6008).

II. ESD Protection Circuit

1. ESD Design Window and ESD Protection Strategy

The ESD protection circuit must not affect the normal operation of internal circuits. As a result, each device has an ESD design window, considering the normal operation state of the internal circuit and the individual devices comprising the internal circuit. If the ESD protection circuit activates in the operation region of the internal circuit, then it will cause the operation signals or supply voltage of the internal circuit to be discharged to the ground, or a propagation delay of the signals can occur. Furthermore, if the internal circuit damage region considering the individual devices comprising the internal circuit is invaded, then the operation of the ESD protection circuit could cause critical damage to the internal circuit. Even if the ESD protection circuit performs protective functions while satisfying the ESD design window, there is still a limited range of current that the protection circuit itself can withstand.

Furthermore, if the ESD protection circuit has too large a resistance, then the rise in voltage before reaching the current limit can damage the internal circuit. Therefore, development of an excellent ESD protection circuit with low on-resistance is needed, while being able to withstand a high ESD current [7]–[8].

Figure 1 shows the ESD design window and the major electrical parameters of an ESD protection circuit. The labels “Vt1” and “It1” in Fig. 1 imply the trigger voltage and current at the moment when the ESD protection circuit is turned on, respectively. The trigger voltage must be smaller than the voltage at which the general devices used in the internal circuit break down or the voltage at which the gate oxide breaks down. The label “Vh” denotes the holding voltage, to prevent latch-up in the normal state, the holding voltage must be greater than the operating voltage of the internal circuit.

Labels “Vt2” and “It2” denote the secondary trigger voltage and current, respectively. The secondary trigger voltage and current are the voltage and current at the point where the ESD protection circuit breaks down.

The trigger voltage of a 3.3 V ESD protection circuit must be lower than the BVdss of the 5 V CMOS device in the design manual to avoid damaging the internal circuit. Furthermore, when the latch-up phenomenon is caused by the low holding voltage of a general SCR protection circuit, which is lower than the operation voltage of 3.3 V, the operation of the internal circuit will be stopped and a large current will be generated through the ESD protection circuit. This can cause thermal runaway, leading to the breakdown of IC devices [9]. To satisfy the ESD design window in Fig. 1, the holding voltage
characteristic must be at least 3.6 V, adding 10% to 3.3 V. This proves that it is possible to mark the ESD design window on the TLP I-V characteristic curve, which was designed in the ESD protection circuit, and to apply it to mobile application ICs that use a 3.3 V I/O.

2. MOS-Triggered SCR-Based ESD Protection Circuit Simulation and TLP Characteristics

The cross section and equivalent circuit of an MOS-triggered SCR-based ESD protection circuit are shown in Figs. 2(a) and 2(b). The structure of the MOS-triggered SCR-based ESD protection circuit is characterized by the low trigger voltage of the SCR structure, achieved by supplying the trigger current through the 2-finger ggNMOS structure. The trigger current (that is, the hole current) is supplied through a metal connection within the source diffusion region of the ggNMOS by adding the P+ diffusion region to the SCR structure. As a result, the avalanche breakdown voltage in the N-well and P-well of the SCR can be lowered, and a lower trigger voltage characteristic can be obtained.

The operation mode consists firstly of the operation by ggNMOS when static electricity is applied to the anode terminal and secondly the operation by the SCR. The bridge P+ diffusion region, which is inserted in the SCR, is connected by metal to the source diffusion region of the ggNMOS and supplies the trigger current from the ggNMOS to the P-well of the SCR. As the voltage increases by the ESD pulse flowing to the anode terminal, the potential at the N-well of the SCR and the drain terminal of the ggNMOS increases. An electron-hole pair is then created by the high electric field at the drain and P-well of the ggNMOS. As a result, a parasitic NPN bipolar path of the ggNMOS is formed, which can be described as the first trigger of the protection circuit. The hole current that was generated after the avalanche breakdown increases the electric potential of the P-well and is then discharged to the P+ tap diffusion region of the SCR through the N+ source diffusion region of the ggNMOS when the electric potential of the P-well becomes higher than the electric potential of the N+ source diffusion region. The difference between the electric potentials of the P-well and the N-well of the SCR then decreases gradually, as a result of the hole current flowing into the SCR.

When the electric field of the SCR N-well and P-well, which are reverse junctions, reaches the critical value, an electron-hole pair is generated by an avalanche breakdown. The generated hole current moves to the P-well region, and the electric potential of the P-well becomes higher than the internal electric field of the P-well/N+ cathode junction. As a result, the two junctions become biased in the forward direction, and the parasitic NPN bipolar (Q2) turns on. The current of the parasitic NPN bipolar (Q2) causes a voltage drop in \( R_{NW} \), causing the parasitic PNP bipolar (Q1) to turn on as well. When all bipolar (Q1, Q2) have been turned on, the second trigger voltage and holding voltage of the protection circuit are formed. The current of the parasitic PNP bipolar (Q1) helps maintain the turn-on state of the parasitic NPN bipolar (Q2). Thus, the static current is discharged with a latch motion that
does not require the supply of bias to the parasitic NPN bipolar (Q2) by the current of the parasitic PNP bipolar (Q1).

Figure 3 shows a graph representing the conventional SCR-based ESD protection circuit through a MOS-triggered SCR-based ESD protection circuit and the TCAD simulation of the electrical characteristic. For this simulation, the structure was designed with TSUPREM4 of SYNOPTYS, and electrical characteristics were analyzed with MEDICI.

The trigger voltage of the MOS-triggered SCR-based ESD protection circuit was about 5.4 V, which is about 20 V lower than the trigger voltage of the conventional SCR-based ESD protection circuit, predicted to be 26 V. The holding voltage of the MOS-triggered SCR-based ESD protection circuit was 1.9 V, which is about 0.75 V higher than the conventional SCR-based ESD protection circuit (1.15 V).

To measure the electrical characteristic of the ESD protection circuit, the TLP was measured. Before designing the ESD protection circuit, the ESD design window was determined considering its relation with the internal circuit. The TLP measurement is a critical element for verifying the appropriateness of the designed ESD protection circuit for the ESD design window to be used [10].

The actual ESD pulse is a direct current (dc) pulse carried out over a short period of time (under 100 ns). If the electrical characteristic measurement method of the ESD protection circuit is used, then the continuation of a high current and voltage for a long time will result in the self-heating of the circuit, making it difficult to obtain accurate measurements. Therefore, a measurement method using a rectangular pulse is required. The most widely used is the TLP measurement method, and it is ideal for the measurement and analysis of the characteristics of the ESD protection circuit, as it can analyze robustness through quasi-static current characteristics and It2.

Figure 4 shows the waveform of the voltage applied to the equivalent circuit of the TLP system and the device under test (DUT). Because a certain voltage is charged through the transmission line and is applied to the DUT through a switch, the pulse width and voltage are adjustable by changing either the length of the transmission line or the initial voltage level. The pulse width and rising time of the square wave applied from the TLP system used for the measurement of the DUT are 100 ns and 10 ns, respectively.

Figure 5(a) shows the layout designed in the 0.18 µm BCD technology of the MOS-triggered SCR-based ESD protection circuit. Figure 5(b) shows the TLP I-V characteristic curve to which the ESD design window was applied, to show its applicability for application in mobile ICs with 3.3 V operating voltage. To apply this to devices with 3.3 V operating voltage, the holding voltage of the ESD protection circuit must be equal to or greater than a 10% margin of increase over the supply voltage, and the region that triggers the core damage must be based on the BVdss 12 V of the 5 V CMOS device.

The TLP I-V characteristic curve showed a similar trend as the simulation results. However, there was a difference between the trigger voltage and holding voltage. This is because the simulation itself does not accurately correspond to real-life technology, and the TLP is an ac characteristic whereas the simulation is a dc characteristic. The appropriateness of the mobile 3.3 V ESD design window was verified through the
Fig. 6. (a) Cross section of MOS-triggered SCR-based ESD protection circuit with floating N+/P+ diffusion regions and (b) simulation structure.

TLP I-V characteristic curve, which is shown in Fig. 6(b). The ESD protection circuit had a low trigger voltage of 6.9 V and a high holding voltage of 4.45 V. However, the on-resistance rose through the diffusion region, which was added for application to the 3.3 V protection circuit. As a result, the effective robustness was limited in the 12 V region of the internal circuit breakdown voltage. The MOS-triggered SCR-based ESD protection circuit had an effective robustness value (It2) of about 4.6 A, but it was limited to 2.8 A due to the 12 V limitation of the core damage region of the ESD design window. The limited effective robustness was increased by changing the on-resistance through the multi-finger structure, which will be described in the next section.

Figure 6(a) shows a cross section of the structure by which the holding voltage characteristic was increased for the 3.3 V ESD protection circuit. Figure 6(b) shows the simulated structure of the ESD protection circuit, including the floating N+/P+ diffusion regions. This removed the N+ region between the N-well and P-well in the SCR region of the 3.3 V ESD protection circuit and induced the avalanche breakdown in the N-well and P-well. Furthermore, it added a floating N+ diffusion region to the N-well region and a floating P+ diffusion region to the P-well region, which caused relative enlargement of the effective base width of the parasitic NPN/PNP bipolar and diminished the current gain compared to the existing value; thus, it raised the holding voltage.

The inducement of an avalanche breakdown in the P-well and N+ diffusion regions of the 3.3 V MOS-triggered SCR-based ESD protection circuit structure through the P-well and N-well increased the trigger voltage by about 1.5 V. The operation mode is identical to that of the 3.3 V MOS-triggered SCR-based ESD protection circuit. The ESD protection circuit including the floating N+/P+ diffusion regions through the current flow lines is shown in Figs. 7(a), 7(b), and 7(c), showing the bias conditions of the protection circuit. Figure 7(a) depicts the state before the trigger. As shown in the figure, there is a leakage current in the silicon bulk and an avalanche breakdown current between the N+ drain diffusion region (anode) of the right-side ggNMOS and the P-well in most cases. Figure 7(b) shows the current flow during the first trigger condition. Most currents flow to the N+ source diffusion region and are injected into the P-well through the P+ tap in the P-well region of the SCR. Figure 7(c) shows the current flow at the moment when the protection circuit discharges the ESD current after the second trigger has
occurred. From this figure, we can see that all the internal parasitic bipolars of the SCR are activated, discharging the ESD current from the anode to the cathode.

The simulation results of the conventional SCR, MOS-triggered SCR-based ESD protection circuit, and MOS-triggered SCR-based ESD protection circuit with floating region are shown in Fig. 8(a), and the turn-on time of the MOS-triggered SCR-based ESD protection circuit (about 2 ns) is faster than that of the conventional SCR (3.3 ns), as shown in Fig. 8(b). From the simulation results, the MOS-triggered SCR-based ESD protection circuit is more suitable than the conventional SCR for quick discharge of the electrostatic energy. The layout of the MOS-triggered SCR-based ESD protection circuit with floating N+/P+ diffusion regions through the 0.18 µm BCD technology is shown in Fig. 9(a), and Fig. 9(b) demonstrates the 1.5 V increase in the holding voltage, from 4.5 V to 6 V, achieved by the added floating N+/P+ diffusion regions, through comparison of the TLP I-V characteristics.

3. Improvement of On-Resistance of MOS-Triggered SCR-Based ESD Protection Circuit

As mentioned, an ESD protection circuit for application in mobile devices using a 3.3 V operating voltage was designed. Electrical characteristics were verified through TCAD simulations, and use of the 0.18 µm BCD technology was analyzed by designing an SCR, a MOS-triggered SCR-based ESD protection circuit, and a MOS-triggered SCR-based ESD protection circuit with floating N+/P+ diffusion regions at the same 100 µm width. However, due to the large on-resistance compared to that of the SCR, the effective robustness value was limited to 4 A or lower at the core damage region of 12 V. This is because the resistance component of the entire protection circuit was increased by including the floating N+/P+ diffusion regions to change the trigger voltage and holding voltage. To compensate, the 2-finger ggNMOS finger of the MOS-triggered SCR-based ESD protection circuit was changed to 12, 14, and 16 fingers so as to decrease the on-
Fig. 10. (a) Layout of 16-finger MOS-triggered SCR-based ESD protection circuit and (b) measured TLP I-V characteristics.

resistance. The layout of the MOS-triggered SCR-based ESD protection circuit is shown in Fig. 10(a), and the TLP I-V characteristics are shown in Fig. 10(b). It was verified that the effective robustness was limited to about 3 A or higher by using a 12-finger (or higher) structure, compared to the protection circuit designed with the MOS-triggered SCR-based ESD protection circuit with a 2-finger structure.

III. ESD Protection Circuit for 20 V Power Clamp

1. Simulation and Operation Characteristics of 20 V SCR-Based ESD Protection Circuit

Figure 11 shows a cross-sectional diagram of the 20 V SCR-based ESD protection circuit with floating N+/P+ diffusion regions. Unlike the conventional SCR, the N-well region includes a floating N+ diffusion region, and the P-well region includes a floating P+ diffusion region. Furthermore, the breakdown voltage of the 20 V SCR-based ESD protection circuit was increased to 20 V or higher.

The depletion region between the N-well and P-well was found to gradually increase through the TCAD simulation (Fig. 12). The depletion region in the “Deep N-well” region, having a low doping region, gradually increased in the order of (a), (b), (c), and (d), and the avalanche breakdown occurred as the expanded depletion region touched or approached the P-well [11].

The gap between the N-well and P-well was optimized to fix the breakdown voltage of 20 V SCR-based ESD protection circuit to 23 V. The 20 V SCR-based ESD protection circuit with the floating N+/P+ diffusion regions has the same operation mode as the SCR, and the base width of the parasitic PNP/NPN bipolar was increased by the addition of the floating region. As a result, the recombination ratio in the base region was increased, and the decreased current gain raised the holding voltage. Figure 13(a) shows the TCAD simulation results obtained by varying the floating N+/P+ diffusion regions to sizes of 5 µm, 10 µm, 15 µm, and 20 µm. The TCAD simulation showed an increase in the holding voltage from 3.3 V to 8.98 V, while the holding voltage characteristics became higher than the conventional SCR protection circuit.
Fig. 13. (a) TCAD simulation results of SCR-based ESD protection circuit with floating N+/P+ diffusion region and (b) simulation setup to measure the turn-on time.

Figure 13(b) shows that the turn-on time of the conventional SCR and SCR-based ESD protection circuit with floating region are equal at 3.3 ns under circuit simulation. To be used as a 20 V ESD protection circuit, it must have a trigger voltage that is lower than the region that can damage the internal circuit, with the BVdss of the 20 V device in the 0.18 µm BCD design manual. Furthermore, it must have a holding voltage that is higher than the operating voltage of 20 V to have immunity to latch-up. The Max It2 was limited to the minimum of 34 V based on the 20 V LDMOS in the design manual. Figure 14(a) shows the layout designed through the 0.18 µm BCD technology. Figure 14(b) shows the ESD design window including the 20 V ESD protection circuit TLP I-V characteristic curve. It demonstrated a trigger characteristic of 28.4 V and a holding characteristic of 23 V. Furthermore, in a single protection circuit, it had a high robustness characteristic of about 8 A but this was limited to 4.5 A due to the 34 V limitation of the internal circuit damage region. The reason for this is the reduced current driving ability due to the increased component of total resistance of the protection circuit by the floating N+/P+ diffusion regions of the N-well and P-well, which were added to increase the holding voltage.

2. Improvement of Characteristics of 20 V SCR-Based ESD Protection Circuit through P-body Layer

A P-body double diffused well (DWELL) layer was added to reduce the gap between the breakdown and trigger voltage of the 20 V SCR-based ESD protection circuit.

Figure 15 shows a cross section of the 20 V SCR-based ESD protection circuit, containing the P-body (DWELL) layer. In Fig. 15, the SCR-based ESD protection circuit with a P-body (DWELL) layer partially includes the P-body (DWELL) region in the P-well region, which has a higher doping concentration than the P-well. The breakdown voltage was decreased to 21 V. In addition, the trigger voltage was lowered by partially adding the P-body (DWELL), which has a lower parasitic resistance than the P-well, and by inducing the N-well and P-body instead of the breakdown voltage of the N-well/
**Fig. 15.** Cross section of SCR-based ESD protection circuit with floating diffusion regions and P-body layer.

**Fig. 16.** (a) Layout of SCR-based ESD protection circuit with floating region and (b) measured TLP I-V characteristics.

P-well in the SCR.

The ESD protection circuit’s on-resistance characteristic was lowered because the resistance component in the discharge path of the entire on-resistance characteristic was decreased. Figure 16(a) shows the layout of the 20 V SCR-based ESD protection circuit with its floating N+/P+ diffusion regions and P-body layer, which was designed through the 0.18 µm BCD technology. Figure 16(b) shows that the trigger voltage was lowered by 1 V from 28.4 V to 27.4 V by the addition of the P-body layer, which was measured through the comparison of the TLP I-V characteristic of the 20 V SCR-based ESD protection circuits, including the P-body (DWELL) layer.

The ESD protection circuit, with a trigger voltage lower than the 34 V of the minimum BVdss of the 20 V LDMOS in the manual, but higher than 22 V, was designed by adding a safety margin of 10% to the supply voltage. The human body model measurement revealed that both the 20 V SCR-based ESD protection circuit with floating N+/P+ diffusion regions and the ESD protection circuit with the added P-body (DWELL) layer satisfied the 8 kV requirement.

However, the actual applicable effective robustness was limited to about 4.5 A, due to the 34 V limitation of the breakdown voltage of the 20 V LDMOS that must be protected by the SCR-based ESD protection circuit with floating N+/P+ diffusion regions. Consequently, a structure that increased the effective robustness to 4.7 A was designed through the addition of a partial P-body layer to the ESD protection circuit, also lowering the trigger voltage by 1 V and reducing the on-resistance.

**IV. Conclusion**

In this paper, SCR-based ESD protection circuits were designed, which are applicable for mobile applications in 3.3 V I/O; notebook adapters and inverters; and LED drivers that use 20 V power clamps. The 3.3 V MOS-triggered SCR-based ESD protection circuit had a trigger voltage of 6.9 V and a holding voltage characteristic of 4.45 V, obtained by inducing a low trigger voltage through a 2-finger ggNMOS. It also included floating N+/P+ diffusion regions that raised the characteristics of the 3.3 V MOS-triggered SCR-based ESD protection circuit having a holding voltage characteristic of 6 V and a trigger voltage characteristic of 8.6 V. It recorded a turn-on time of 2 ns, which is faster than that of the conventional SCR ESD protection circuit (3.3 ns). The number of fingers of the 2-finger ggNMOS was changed to 12, 14, and 16 to improve the on-resistance, which had become larger than those of the diffusion regions added to improve the trigger voltage and holding voltage characteristics.

To apply the SCR structure to a 20 V power clamp, the breakdown voltage of the protection circuit was fixed to 23 V, and the floating N+/P+ diffusion regions were increased to 23 V through an optimization of the holding voltage. The breakdown voltage was lowered to 21 V by the addition of a partial P-body layer, which lowered the trigger voltage from 28.4 V to 27.4 V.
From the results, it can be concluded that the 3.3 V I/O and 20 V power clamp ESD protection circuits are appropriate for the ESD design window and that they are expected to further improve the reliability of the low- and high-voltage ICs, compared to the conventional SCR-based ESD protection circuit.

References


Jin Woo Jung received his MS degree in electronic and electrical engineering from the Department of Electronic and Electrical Engineering, Dankook University, Yongin, Rep. of Korea, in 2012. He is currently working toward his PhD degree in electronic and electrical engineering at Dankook University. His research interests include power semiconductor devices and electrostatic discharge protection circuit design.

Yong Seo Koo received his BS, MS, and PhD degrees in electronic engineering from Sogang University, Seoul, Rep. of Korea, in 1981, 1983, and 1992, respectively. He joined the Department of Electronics and Electrical Engineering, Dankook University, Yongin, Rep. of Korea, as a professor in 2009. His current research interests include power semiconductor devices, power management integrated circuits, and electrostatic discharge protection circuit design.