Nonvolatile Memory Characteristics of Double-Stacked Si Nanocluster Floating Gate Transistor


Abstract—We have studied nonvolatile memory properties of MOSFETs with double-stacked Si nanoclusters in the oxide-gate stacks. We formed Si nanoclusters of a uniform size distribution on a 5 nm-thick tunneling oxide layer, followed by a 10 nm-thick intermediate oxide and a second layer of Si nanoclusters by using LPCVD system. We then investigated the memory characteristics of the MOSFET and observed that the charge retention time of a double-stacked Si nanocluster MOSFET was longer than that of a single-layer device. We also found that the double-stacked Si nanocluster MOSFET is suitable for use as a dual-bit memory.

Index Terms—Double-stacked Si nanocluster, LPCVD, dual-bit memory, floating gate nonvolatile memory

I. INTRODUCTION

Nanocrystal-based charge-storage memory devices have recently attracted much attention because of their potential to overcome the limitations of current floating gate memories with poly silicon or silicon nitride film as their charge storage layers. The nanocrystal memory devices offer several advantages, such as short program/erase times and low program/erase voltages, including the potential to use a very thin tunnel oxide without sacrificing non-volatility. Forming the thin tunnel oxide layer is the first step toward enabling quick and efficient charge transfer to and from the floating gate. There are other advantages as well. The nanocrystal memory devices suffer less from the drain-induced-barrier-lowering, so that absence of the drain-to-floating gate coupling derives that these memory devices have intrinsically better punchthrough characteristics than that of conventional one. However, current nanocrystal memory devices have a relatively low density of charge storage, and consume a great deal of power to operate on/off, so these problems need to be solved for that they can be used in practical applications.

Recently, the use of memory devices with multi-level charge storage were suggested in various literatures [1, 2], where they fabricated the multi-level memory devices by using low energy plasma immersion implantation and post annealing. Here, we suggest the use of the Low Pressure Chemical Vapor Deposition (LPCVD) method in order to fabricate a multi-level charge storage memory device. This method is a promising way to mass-produce such memory devices, because it is compatible with current Si processing technology. In the multi layer Si nanocrystal structures, multi-bit operation can be performed by adjusting the number of Si nanocrystal layers and the control oxide thickness. The multi-bit operation increases the memory capacity over the conventional single-bit device, as it creates two different transistor operations out of one transistor. In addition, since the charge leakage between the upper Si nanocrystal layer and the channel can be suppressed because of the Coulomb repulsion from the lower Si nanocrystal layer, the retention time can be enhanced.

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II. EXPERIMENT

The MOSFET with Si nanocluster floating gate layers were fabricated on p-type (100) Unibond SOI wafers with a 100-nm thick top Si layer and a 200-nm thick buried oxide layer. The active Si region, which consists of the channel and the source/drain, was defined by photolithography and reactive ion etching. A 5 nm-thick SiO$_2$ film was thermally grown in a dry oxidation furnace to make a tunneling oxide layer. We then formed Si nanoclusters on the tunneling oxide layer by using the pulse-type gas-feeding technique in the LPCVD system. The details of pulse-type gas-feeding technique were described in the previous work. [3] A pure SiH$_4$ gas was used as a source gas. A double-stacked structure of Si nanocluster was produced by depositing a 10-nm thick SiO$_2$ using the LPCVD at 400 °C with mixed gases of SiH$_4$ and O$_2$, followed by an additional deposition of the Si$_2$H$_6$ gas. The surface density of the Si nanoclusters that had an average diameter of 7 nm was approximately 7 x 10$^{11}$ cm$^{-2}$. The nanocluster stacks were then covered by a control oxide layer that was deposited with SiH$_4$ and O$_2$ at 400 °C by using an LPCVD method. We deposited a poly-Si layer for a gate electrode on the control oxide with SiH$_4$ at 640 °C, and the gate electrode was then patterned. Finally, the phosphorus plasma doping method was used at 500 °C to carry out source/drain/gate doping.

![Fig. 1. A schematic diagram MOSFET with double-stacked Si nanocluster floating gate.](image)

III. RESULTS AND DISCUSSION

Fig. 2 demonstrates the program/erasing behaviors under different gate voltages with various pulse widths ranging from 1 µs to 1 s. In Figure 2 (a), two plateaus were observed, which corresponded to the threshold voltages of -0.4 V and 0.3 V. The increment of the threshold voltage in the second shift than in the first one along the electron charging time. Threshold voltage shifts of 1.0 V and 1.7 V were achieved at 18 V for 1 ms and 100 ms, respectively.

For a simple MOSFET structure with double-stacked floating gate, the threshold voltage shift was correlated with the dielectric property and thickness of the control oxide, and trapped charge. [4, 5]

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\Delta V_{th} = \frac{\varepsilon_m \varepsilon_0}{\varepsilon_{Si}} (d_1 + \frac{\varepsilon_m}{2\varepsilon_{Si}}r_{ox} + d_2 + \frac{\varepsilon_m}{2\varepsilon_{Si}}r_{ox})
$$

where $\Delta V_{th}$ is the threshold voltage shift, $n_{dot}$ is the density of the nanocrystals, $d_N$ is the control oxide thickness of the Nth layer, $\varepsilon_m$ is the permittivity of the control oxide, and $r_{ox}$ was the diameter of the nanocrystals.

Each of the Si nanocluster layers has a different control oxide thickness. The control oxide thickness of the first and second layer was 40 nm and 30 nm, respectively, and the diameter of Si nanoclusters was 7 nm. We assumed that...
each layer had the same density of the Si nanoclusters, i.e., it had the same trap charge. We estimated from equation (1) that the respective threshold voltage shifts were proportional to 41.15:71.15 = 1:1.73. This ratio was nearly the same as the measured values, where the position of the two plateaus showed a ratio of 1:1.7. The result shows the presence of a Double-Bit Cell in which the first layer and the second layer are programmed separately.

As shown in Fig. 2 (b), the threshold voltage shift caused by the hole charging is different from that caused by the electron charging. The memory window of the hole charging (~2.4 V) is larger than that of the electron charging (~1.7 V). The increased memory window in the hole charging is thought to result from the larger shift of the energy level in the conduction band than that in the valence band by the quantum confinement effect. [6] Therefore, the tunneling barrier height for the stored electron is small compared to that for the stored hole, which may cause a long retention time for the stored holes. For the hole charging, two plateaus were observed which are located at -1.7 V and -3.8 V, but the extent of the threshold voltage shift was different from that of the electron charging. As we used p-type Si substrates, the tunneling barrier height is higher for the hole transfer than with the electron transfer to the Si nanoclusters. To inject holes into the valence band of Si nanoclusters, a higher voltage is required than that needed to inject electrons, thus hole charging may commence at the second layer before charging the first layer fully.

We investigated the effect of the double-stacked structure on the charge retention by comparing the threshold voltage changes of the single layer and of the double layer devices after they had been fully charged. The threshold voltage change with time is shown in Fig.

![Fig. 3. Retention characteristics for the double-stacked Si nanocluster floating gate transistor and single layer floating gate transistor.](image)

3. We found that the charge retention of double layer memory was better than that of the single layer memory. The increased retention time of the double layer memory is explained by the suppression of the charge leakage that is caused by the Coulomb repulsion from the lower nanocluster stack between the upper nanocluster stack and the channel.

The endurance characteristics of the double-stacked Si nanocluster floating gate MOSFET devices are shown in Fig. 4. The gate voltage pulse height and width for program/erase were ±18 V and 100 ms, respectively. The drain voltage was set to V_D = 50 mV. At room temperature, a drift of 0.5 V in the program/erase threshold voltage was observed after 10^4 program/erasing cycles. The drift-up in the threshold voltage is attributed to the electron trapping in the oxide layer.

IV. SUMMARY

In summary, MOSFETs with double-stacked Si nanoclusters were fabricated. The performance of the double layers memory devices was characterized by measuring the threshold voltage under various gate bias conditions. The plateaus in the threshold voltage shift suggested the possibility of the Double-Bit operation. Because of the Coulomb repulsion from the lower nanocluster stack, charge leakage in the upper nanocluster stack was suppressed and the charge retention of the double layer memory was better than that of a single layer memory.

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REFERENCES


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