Investigation of Frequency Dependent Sensitivity of Noise Figure on Device Parameters in 65 nm CMOS

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Abstract—We have investigated the noise sensitivity of low noise amplifier (LNA) at different frequencies. This noise sensitivity analysis provides insights about noise parameters and is very beneficial for making appropriate design trade-offs. From this work, the circuit designer can choose the adequate noise parameters tolerances.

Index Terms—Noise sensitivity, CMOS, low noise amplifier, LNA, optimization

I. INTRODUCTION

RF circuit design is difficult in advanced technology because of process variability and lack of accuracy of models. Therefore, we should take such unpredictable process variations into account during the circuit design stage in deep submicron technology. Noise sensitivity analysis could provide the design approach to reduce these variations for better circuit design. A low-noise Amplifier (LNA) is one of the most critical circuit blocks in a wireless transceiver. As the first stage in the receiver architecture, noise figure of LNA dominates overall noise performance of the system [1]. Therefore, we analyzed frequency dependent sensitivity of noise figure of LNA. For more accuracy, we adopted small signal equivalent circuit with gate-to-drain capacitance consideration and analytic noise model of MOSFET. This work is done by measurement data of 65 nm CMOS devices.

II. NOISE FIGURE OF LNAs

Conventional LNAs schematic is shown in Fig. 1. And small signal equivalent circuit with C_{gd} is shown in Fig. 2.

As the technology is scaled down, the effect of the C_{gd} is not ignored any more. From that equivalent circuit, noise figure equation can be derived as below [2]. The channel thermal noise, S_{ch}, is analytically modeled and predicts the measured channel thermal noise well [3,4].

\[ NF = \frac{R_s}{R_g} + \frac{S_{ch}}{4kT} \left( f \frac{R_1 f_1}{f} \right)^2 + \frac{S_{ch}}{4kT} \left( f \frac{R_2 f_2}{f} \right)^2 \]

(1)

Fig. 1. Schematic of a conventional cascode LNA.

Fig. 2. Small signal equivalent circuit of cascode LNA with C_{gd}.
\[ NF - 1 = \left( \frac{R_t}{R_{stg}} + 4R_{stg} \right) \frac{\alpha S_{\delta t}}{\gamma} + 4R_{stg} \frac{\beta S_{\delta t}}{\gamma} \] (2)

\[ S_{vd} = 4kT \left( \frac{m}{V_G - V_o} + \frac{mV_o}{V_G(V_G - V_o)} \right) \] (3)

where \( V_G = V_{GS} - V_{TH}, V_o = I_{DS}/W/C_{oss}V_{TH}, \) and \( m \) is the body-effect coefficient. \( R_t \) is sum of parasitic resistance of gate and source inductor \( (R_{Gt}, R_s) \), gate electrode resistance \( (R_{Ge}) \) and source resistance \( (R_s) \). The equation (1) is extended to equation (2) with \( C_{stg} \) consideration. And parameters such as \( \alpha, \beta \) and \( \gamma \) are as shown below where \( C_{gs} = C_{gst} + C_{gso} \) and \( R_{stg} = R_t + R_{stg} \) [2].

\[ \alpha = \left[ \frac{1}{C_{gst}} + \left\{ \frac{1}{C_{gs}} + \frac{R_{gs}}{1 + \frac{R_{gs}}{C_{gs}}} \right\} \right]^2 \] (4)

\[ \beta = \left[ \frac{1}{C_{gso}} + \left\{ \frac{1}{C_{gs}} + \frac{R_{gs}}{1 + \frac{R_{gs}}{C_{gs}}} \right\} \right]^2 \] (5)

\[ \gamma = \left( \frac{R_{stg}}{C_{gst} + C_{gs}(1 + \frac{R_{gs}}{C_{gs}})} \right)^2 \] (6)

There are two noise terms with different noise sources; resistor source and transistor source [4]. Therefore, we could classify parameters as two noise sources. Q-factor and \( L_g \) are related to resistor noise term and \( V_{GS} \) width of device, \( C_{oss}, C_{vat} \) and drain current are related to transistor noise term. And other parameters such as \( C_{gs}, C_{bst}, \) \( \alpha, \beta, \gamma \) are multiplied with noise terms. Since there are dominant noise terms at different frequency, we could obtain the sensitivity of these parameters. As frequency increases, \( 1/\alpha C_{gs} \) decreases and \( L_g \) and its parasitic resistance get smaller. Therefore, resistor noise term decreases while the transistor noise term increase as \( f_i \) increases in simplified noise figure equation (1). As a result, parameters related to transistor noise term would be more sensitive than others at high frequency while parameters related to resistor noise term are more sensitive at low frequency [5].

### III. Optimization with FoM and Sensitivity Analysis

At higher frequency, we generally use smaller device width. Since the noise sensitivity varies as width of device changes, we should first determine the optimum width of device and bias point of LNA for more similarity to real design situation. The figure of merit (FoM) represented as below is index of performance of LNA [6].

\[ \text{FoM}_{LNA} = \frac{G \cdot f}{(NF - 1) \cdot P} \] (7)

where \( G \) is signal power gain in absolute unit, \( NF \) is noise factor in absolute unit, \( P \) is power dissipation, and \( f \) is operation frequency. We can obtain the FoM of LNA using following gain equation and FoM optimization for 17 GHz is shown as Fig. 3-(a), (b) where \( f_{T1} \) and \( f_{T2} \) are cut-off frequency of M1 and M2 transistor.

![FoM Optimization of LNAs](image)

**Fig. 3-1. FoM Optimization of LNAs (a) width optimization and (b) gate bias optimization for 10 GHz.**
Fig. 3-2. FoM Optimization of LNAs (a) width optimization and (b) gate bias optimization for 17 GHz.

\[ G = \frac{1}{4} \left( \frac{f_{11}}{f} \right)^2 \left( 1 + \left( \frac{f}{f_{72}} \right)^2 \right) \]  \hspace{1cm} (8)

We can also obtain the FoM of LNA for 10 GHz and 24 GHz for comparison. Optimum device width of 102.4 μm for 10 GHz, 61.6 μm for 17 GHz and 40.8 μm for 24 GHz were obtained at \( V_{gs} = 0.65 \) V. Fig. 4 shows the effect of \( S_{d1} \) on noise figure. The ±50% variation of \( S_{d1} \) makes deviation of 0.35 dB at 10 GHz, 0.56 dB at 17 GHz, 0.76 dB at 24 GHz. At higher frequency, channel thermal noise is sensitive on noise figure and \( S_{d1} \) is more sensitive than \( S_{d2} \) for all frequency range. However, the effect of \( S_{d2} \) on noise figure is increased more rapidly than that of \( S_{d1} \).

To invest frequency dependent sensitivity of other design parameters, all parameters have been changed by 10% of change of each parameter. Gate inductor, \( Q \) factor, \( C_{gs1}, C_{gd1}, C_{gs2}, g_{m1} \) and \( g_{m2} \) are considered as important parameters on noise figure.

The nominal values of noise figure are 1.96 dB at 10 GHz, 2.5 dB at 17 GHz, 3.58 dB at 24 GHz. These results provide which parameter should be considered firstly for noise tolerable design.

As we expected, parameters related to resistor noise term such as \( L_{g} \) and \( Q \)-factor are more sensitive at lower frequency. And parameters multiplied with noise terms such as \( C_{gs}, C_{pd} \) and \( g_{m} \) are more sensitive at higher frequency.

From these results, it is found that parameters which are extracted from DC model such as \( V_{th}, I_{d} \) and \( g_{m} \) are important for all frequency and should be modeled carefully for accurate noise expectation. And parameters related to resistor noise term are important at low frequency while parameters multiplied with transistor noise term are important at high frequency.
Fig. 4. NF deviation vs. parameters for $S_{21}$ at (a) 10 GHz, (b) 17 GHz and (c) 24 GHz.

IV. CONCLUSIONS

In this paper, we designed LNA with FoM optimization and analyze noise sensitivity of LNAs for frequency. Parameters extracted from DC model such as $V_n$, $I_0$ and $g_m$ should be accurate to reduce the unpredictable variation for all frequency. And parameters related to resistor noise term are more sensitive at low frequency while parameters multiplied with transistor noise term are more sensitive at high frequency. From this work, circuit designers can determine which parameters are important and focused on. In addition, parasitics which effect on important parameter should be considered firstly.
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REFERENCES


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Jong Duk Lee was born in Young-chun, Kyungpook, Korea. He received the B.S. degree in physics from Seoul National University in 1966. He received the Ph.D. degree from the Department of Physics at the University of North Carolina at Chapel Hill in 1975. He served at the Military Communication School as a ROTC officer from 1966 to 1968. He then worked at the Engineering College of Seoul National University as a teaching assistant in the Department of Applied Physics until 1970. He was an Assistant Professor in the Department of Electronics Engineering at Kyungpook National University from 1975 to 1978. In 1978, he studied microelectronic technology in HP-ICL at Palo Alto, CA, USA, and soon afterward worked for the Korea Institute of Electronic Technology (KIET) as the director of the semiconductor division. He established the KIET Kumi Facility and introduced the first polysilicon gate technology in Korea by developing 4K SRAM, 32K and 64K Mask ROM's, and one-chip 8-bit microcomputer.

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