A Rail-to-Rail Input 12b 2 MS/s 0.18 μm CMOS Cyclic ADC for Touch Screen Applications

Hee-Cheol Choi*, Gil-Cho Ahn*, Joong-Ho Choi**, and Seung-Hoon Lee*

Abstract—A 12b 2 MS/s cyclic ADC processing 3.3 Vp-p single-ended rail-to-rail input signals is presented. The proposed ADC demonstrates an offset voltage less than 1 mV without well-known calibration and trimming techniques although power supplies are directly employed as voltage references. The SHA-free input sampling scheme and the two-stage switched op-amp discussed in this work reduce power dissipation, while the comparators based on capacitor-divided voltage references show a matched full-scale performance between two flash sub ADCs. The prototype ADC in a 0.18 μm 1P6M CMOS demonstrates the effective number of bits of 11.48 for a 100 kHz full-scale input at 2 MS/s. The ADC with an active die area of 0.12 mm² consumes 3.6 mW at 2 MS/s and 3.3 V (analog)/1.8 V (digital).

Index Terms—Analog-to-Digital Converter (ADC), CMOS, cyclic, low offset, rail-to-rail.

I. INTRODUCTION

Highly power efficient analog-to-digital converters (ADCs) based on oversampling, successive approximation register, and cyclic architectures have been commonly employed for audio and sensor applications such as voice recording, micro electro mechanical systems, power management units, and touch screen. Those audio and sensor ADCs operate at a several kS/s to MS/s rate with low power and small area [1]. As a required system resolution goes beyond 8b, the over-sampling architecture shows the highest power efficiency with the advantage of reduced anti-aliasing requirements [2]. In sensor applications, however, events occur sporadically and input nodes may acquire data only once before having to react. As a result, the conventional Nyquist acquisition capability is preferred. Particularly in X-Y position detectors for a touch screen interface, the cyclic ADC offers the best trade-off between resolution, conversion rate, and flexibility.

On the other hand, gain and offset errors of the cyclic ADC need to be strictly limited to reduce a position detection error in touch screen applications [3, 4]. The major gain error is coming from a finite operational amplifier (op-amp) gain in the input sample-and-hold amplifier (SHA), while the offset error is caused by device mismatches in a differential input pair of the op-amp and passive/active elements of the on-chip reference voltage generator. In the single-ended input signal processing, additional offsets originate from the mismatch of a signal common voltage (VCOM) applied to the differential input pair of the op-amp converting a single-ended input signal into a differential output signal.

In this work, a two-stage cyclic architecture is employed considering the required data conversion rate of 2 MS/s and data output latency of 3 clock cycles. The proposed SHA-free input sampling, passive device-free voltage reference, low-offset multiplying D/A converter (MDAC) switching schemes convert single-ended rail-to-rail input signals into 12b digital codes with minimized gain and offset errors [5].

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* Dept. of Electronic Engineering, Sogang University, #1 Sinseol-Dong, Mapo-Gu, Seoul 121-742, Korea, TEL: +82-2-705-8912, FAX: +82-2-715-6129
** Dept. of Electrical and Computer Engineering, University of Seoul, Jeonnong-Dong, Dongdaemun-Gu, Seoul, Korea
E-mail: gcahn@sogang.ac.kr
II. ADC ARCHITECTURE

The proposed 12b 2 MS/s CMOS ADC based on a two-stage (2.5b/stage) cyclic architecture consists of two
MDACs, two flash ADCs, reference current and voltage
senders, a clock generator, and a digital correction
logic (DCL) block, as shown in Fig. 1. The two-stage
cyclic architecture optimizes power dissipation, chip
area, and data output latency at a target resolution of 12b
and a sampling rate of several MS/s.

The non-overlapped clock phases and recycling
control signals are generated on chip from a single
master input clock. The proposed ADC needs 3 clock
cycles to produce a full single 12b binary output corre-
sponding to an analog input. The ADC employs a SHA-
free input sampling scheme simultaneously to achieve
low power and high signal-to-noise ratio (SNR) with the
same input capacitance by eliminating one of the thermal
noise sources in the analog signal path [6]. The two
MDACs use power supply voltages, VDD and VSS, as
reference voltages, while the flash ADCs employ resistor-
divided reference voltages, REFT and REFB. As illustrated
in Fig. 1, analog functional blocks such as the MDACs,
flash ADCs, and reference generators are designed with
3.3 V-based thick-gate oxide devices, while the clock
generator and DCL are implemented with 1.8 V-based
thin-gate oxide devices. Digital level shifters are located
between 3.3 V and 1.8 V functional blocks.

![Fig. 1. Proposed 12b two-stage cyclic ADC.](image)

III. CIRCUIT IMPLEMENTATION

A. MDAC1 Operation

In conventional ADCs, the required top and bottom
reference voltages are generated approximately at 3/4
and 1/4 levels of a full-scale input along with offset
ersors caused by passive or active element mismatches in
the internal voltage generator [7]. On the other hand, the
proposed MDACs directly employ two power supply
voltages, VDD and VSS, as reference voltages corre-
sponding to the maximum and minimum levels of a rail-
to-rail input, respectively. Thus, a very high full-scale
signal matching accuracy is obtained between the ADC
and the touch screen sensor by eliminating any extra
devices for reference voltage generation. Two inaccurate
reference voltages, REFT and REFB, only for the flash
ADCs are produced from a resistor string with a rela-
tively relaxed accuracy requirement of 2.5b in this ADC.

The proposed sampling scheme of the MDAC1 is
shown in Fig. 2 with the front-end analog MUX (AMUX) of Fig. 1. During the input sampling mode, the
upper capacitor array samples a single-ended input
signal, VIN, while the lower capacitor array samples
reference voltages, VDD or VSS, instead of a signal
common, VCOM. The proposed input sampling network
produces a stable common-mode signal by connecting a
half of the sampling capacitors to VDD and the other
capacitors to VSS. As a result, the conventional MDAC offset
effects due to the inaccurate VCOM do not exist. During
the next amplifying mode, the MDAC1 amplifies a
residue voltage, which is the difference between a
sampled input and a reconstructed analog signal from a
digital code of the flash ADC. The specific amplified
residue voltage from Fig. 2 is obtained with a switching
procedure as described in Table 1, and the normalized
residue plot of the MDAC1 is illustrated in Fig. 3. The
proposed SHA-free circuit also reduces finite op-amp gain
error, chip area, and power dissipation simultaneously
with the increased SNR since extra op-amps, sampling
capacitors, and switches for the SHA do not exist.

<p>| Table 1. Mdac1 Capacitor Array Connection During Residue Amplification. |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|</p>
<table>
<thead>
<tr>
<th>FLASH Output</th>
<th>CT0</th>
<th>CT1</th>
<th>CT2</th>
<th>CT3</th>
<th>CT4</th>
<th>CT5</th>
<th>CT6</th>
<th>CT7</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>VCOM</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VDD</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>001</td>
<td>VCOM</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VDD</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>010</td>
<td>VCOM</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VDD</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>011</td>
<td>VCOM</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VDD</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>100</td>
<td>VCOM</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VSS</td>
<td>VDD</td>
<td>VDD</td>
<td>VDD</td>
</tr>
</tbody>
</table>

![Diagram](image)
B. Two-Stage Switched Op-Amp

All of the two MDACs in Fig.1 have a two-stage op-amp topology to achieve the required DC gain and the output swing margin sufficient for a 12b accuracy as shown in Fig. 4.

The folded-cascode architecture with an NMOS input pair in the first stage amplifier primarily achieves a high DC gain while the common-source topology with a tail current source in the second stage amplifier obtains a high output swing. The two-stage op-amp performs an offset cancellation with a closed-loop sampling technique [8]. During the sampling mode, the inputs (INT and INC) and the first stage outputs (OC1 and OT1) are connected in a unity-gain feedback by switch transistors, M3 and M4, to overcome the bandwidth reduction due to the closed-loop sampling scheme. Moreover, the proposed two-stage op-amp uses cascoded compensation and switched op-amp power-reduction techniques to reduce power consumption and active area simultaneously [9, 10]. It is noted that the dynamic common-mode feedback (CMFB) circuit proposed in the second stage amplifier consists of only two capacitors and three switches. The proposed CMFB circuit requires a half the components compared to the conventional switched-capacitor based CMFB circuit [11].

C. Capacitor-Divided Comparator

The flash ADCs are based on a capacitor-divided (C-DIV) comparator instead of a conventional resistor ladder-based comparator, as shown in Fig. 5 (a). The top schematic of the proposed C-DIV based flash ADC is illustrated in Fig. 5 (b). With the proposed latched comparator, all the flash ADCs are free from having a resistor divider, which can cause a gain error between flash sub ADCs due to a voltage drop of reference voltages through interconnection line currents. Each input in the proposed comparator of Fig. 5 consists of two separate capacitors, and the capacitors are connected only to the top and bottom reference voltages, REFt and REFb, selectively. There is no resistor connected to the references.
increasing input frequencies at a sampling frequency of 2 MHz. As shown in Fig. 9, the prototype ADC maintains a SNDR and SFDR exceeding 70 dB and 80 dB with input frequencies increased to 200 kHz. The input signal of the ADC for typical touch screen applications is a sampled data type rather than a sine wave. Considering this point, the proposed ADC employs the closed-loop sampling scheme in the MDAC1 to reduce the offset error of an amplifier, and the bandwidth of the related input sampling network is optimized at 300 kHz. As a result, the input signal bandwidth of the ADC is restricted to about 300 kHz in the evaluation stage. The measured SNDR at a frequency close to the Nyquist rate is degraded to below 50 dB.

The prototype cyclic ADC with the proposed reference scheme demonstrates as low top and bottom offset errors as 0.77 LSB and 0.35 LSB, respectively, which are less than 1 mV. The figure of merit (FoM), defined as Power/(2^SNDR×fs), is 0.63 pJ/conversion-step. The overall ADC performance is summarized in Table 2.

Fig. 5. Flash ADC: (a) Capacitor-divided latched comparator and (b) top schematic of the proposed 2.5b flash ADC.

**IV. MEASURED PERFORMANCES**

The two-stage cyclic prototype ADC is implemented in a 0.18 μm single-poly six-metal CMOS process. It consumes 3.6 mW at a 2 MS/s rate with 3.3 V and 1.8 V power supplies used for analog and digital circuit blocks, respectively.

The active die area is 0.12 mm² (≈330 μm × 365 μm), as shown in Fig. 6. As illustrated in Fig. 7, the measured differential non-linearity (DNL) and integral non-linearity (INL) are within ±0.25 LSB and ±0.69 LSB, respectively. At a conversion rate of 2 MS/s, the measured signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 70.9 dB and 81.7 dB, respectively, with a 100 kHz and 3.3 Vp-p input, as shown in Fig. 8.

The SNDR and SFDR of Fig. 9 are measured with
with an active die area of 0.12 mm², and demonstrates the effective number of bits of 11.48 at 2 MS/s.

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REFERENCES


V. CONCLUSIONS

This work proposes a rail-to-rail input 12b 2 MS/s CMOS cyclic ADC for a touch screen interface. The proposed ADC shows a measured DNL and INL of ±0.25 LSB and ±0.69 LSB, and achieves as low top and bottom offsets as 0.77 LSB and 0.35 LSB levels with a single-ended 3.3 Vp-p input signal, respectively. The prototype ADC shows a power dissipation of 3.6 mW


Hee-Cheol Choi was born in Seoul, Korea. He received the B.S., M.S., and Ph.D. degrees in Electronic Engineering from Sogang University, Seoul, Korea, in 1994, 1996, and 2009. From 1996 to 2006, He worked as a senior engineer at Samsung Electronics. He is currently a senior engineer of Aptina Korea. His work focuses mainly on sensor chip design and his current interests are high-resolution low-power CMOS data converters and analog front ends for video signal processing.

Gil-Cho Ahn received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical engineering from Oregon State University, Corvallis, in 2005. From 1996 to 2001, he was a Design Engineer at Samsung Electronics, Kiheung, Korea, working on mixed analog & digital integrated circuits. From 2005 to 2007, he was with Broadcom Corporation, Irvine, CA, working on AFE for digital TV. Currently, he is an Assistant Professor in the Department of Electronic Engineering, Sogang University. His research interests include high-speed, high-resolution data converters and low-voltage, low-power mixed-signal circuits design. Dr. Ahn received the Analog Devices Outstanding Student Designer Award in 2003.

Joongho Choi was born in Seoul, Korea, in 1964. He received the B.S. and the M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1987, 1989, respectively, and Ph. D. degree in electrical engineering from University of Southern California, California, in 1993. His Ph. D. dissertation focused on the analog-digital VLSI neuron-processors for signal processing and communication. From 1993 to 1996, he worked in IBM T. J. Watson Research Center, NY in USA, where he made researched in integrated GaAs receiver for optical interconnection systems and high-performance sigma-delta A/D converter, compact low-power VLSI transceiver for wireless communication. In 1996, he joined with the University of Seoul, Seoul, where he is Professor in the Department of Electrical & Computer Engineering. His research area is the design of high performance analog integrated circuits.

Seung-Hoon Lee received the B.S. and M.S. degrees with honors in Electronic Engineering from Seoul National University, Seoul, Korea, in 1984 and in 1986, respectively, and the Ph.D. degree in Electrical and Computer Engineering from the University of Illinois, Urbana-Champaign, in 1991. From 1990 to 1993, he was with Analog Devices Semiconductor, Wilmington, MA, as a Senior Design Engineer. Since 1993, he has been with the Department of Electronic Engineering, Sogang University, Seoul, Korea, where he is now a Professor. He has been serving as the chief editor of the IEKE Journal of Semiconductor Devices, Circuits, and Systems and a TPC member of many international and domestic conferences including the IEEE Symposium on VLSI Circuits. His current interest is in the design and testing of high-resolution high-speed CMOS data converters, CMOS communication circuits, integrated sensors, and mixed-mode integrated systems.