Reliability Characteristics of La-doped High-k/Metal Gate nMOSFETs


Abstract—The reliability of hafnium oxide gate dielectrics incorporating lanthanum (La) is investigated. nMOSFETs with metal/La-doped high-k dielectric stack show lower $V_{th}$ and $I_{gate}$, which is attributed to the dipole formation at the high-k/SiO$_2$ interface. The reliability results well correlate with the dipole model. Due to lower trapping efficiency, the La-doping of the high-k gate stacks can provide better PBTI immunity, as well as lower charge trapping compared to the control HfSiO stacks. While the devices with La show better immunity to positive bias temperature instability (PBTI) under normal operating conditions, the threshold voltage shift ($\Delta V_{th}$) at high field PBTI is significant. The results of a transconductance shift ($\Delta G_m$) that traps are easily generated during high field stress because the La weakens atomic bonding in the interface layer.

Index Terms—La-doped high-k/metal gate nMOSFETs

I. INTRODUCTION

High-k gate dielectrics have been studied as alternative gate dielectrics for the 45 nm technology nodes and beyond to replace conventional SiO$_2$ or silicon oxynitrides (SiO$_x$N$_y$) and have been successfully implemented in CMOS integrations [1, 2]. Hf-based oxides, including HfO$_2$ and HfSiO$_x$, have been regarded as promising candidates for high-k dielectrics because of their excellent thermal stability with Si. Furthermore, the mobility of HfSiON devices, which was underestimated due to transient charging during conventional characterization, has improved significantly by dielectric stack optimization based on better understanding of transient charging behaviors in high-k [3-6].

In conjunction with high-k dielectrics, a band-edge metal solution for n- and pMOSFETs is being pursued because it is known that polySi/high-k stacks are limited by dopant penetration, inversion oxide thickness ($T_{inv}$) scalability, threshold voltage ($V_{th}$) controllability by Fermi-level pinning, and poor reliability [7-11]. Various attempts have been made in material screening to find proper band-edge electrode materials [8, 12, 13].

Besides pursuing a band-edge metal solution, a simple rare-earth metal doping technique has been proposed to modulate $V_{th}$ [14-17]. Among various rare-earth metals, lanthanum has been demonstrated as a strong candidate for nMOSFETs because of its low $V_{th}$, good carrier mobility, good EOT scaling, and positive bias temperature instability (PBTI). During a high temperature dopant activation step, electropositive La that has diffused into the high-k/SiO$_2$ interface forms a dipole, which shifts the band offset and thereby the effective work function (EWF) of the electrode. To explain the $V_{th}$/flatband voltage ($V_{fb}$) modulation HfO$_2$ or HfSiO incorporating La, various models were proposed, such as a positive charge by oxygen vacancy and interface dipoles [15-20]. Unlike the $V_{th}/V_{fb}$ modulation caused by additional positive charge generation/increase in the dielectric, devices with La show excellent carrier mobility due to the short range of the dipole electric field [15, 16].
Thus, HfO$_2$ gate dielectric incorporating La seems to be a strong candidate for future nMOS dielectrics, but the effects of the La-induced dipole on device performance and dielectric reliability have not been studied thoroughly. Reliability studies of high-k dielectrics are focusing on understanding mechanisms of how and where defects are generated using various characterization methods [3, 21-27] and it is reported that interface trap generation rather than the bulk high-k layer is very crucial to dielectric reliability [28, 29]. In this work, therefore, we investigate the reliability of nMOSFETs with HfO$_2$ dielectrics that incorporate La, whose device performance and $V_{th}$ are suitable for future technology node applications. We especially focus on how incorporating La into the interfacial layer affects dielectric reliability.

## II. EXPERIMENTAL

Transistors were fabricated using a gate-first integration flow. Hf-silicate films with different SiO$_x$ concentrations were deposited by atomic layer deposition (ALD). A molecular beam deposition (MBD) process was employed to deposit an ultra thin LaO$_x$ cap on the high-k film before depositing the metal gate electrode. Post high-k deposition treatments included a post-nitridation anneal. Mobility was extracted from 10 μm x 1 μm transistors using the NCSU CVC and mob2d models [30]. For comparison, control HfSiO devices were fabricated without the LaO$_x$ cap. The equivalent oxide thicknesses (EOTs) for the sample devices were in the 0.85 ~ 1.02 nm range (Table 1).

<table>
<thead>
<tr>
<th>SiO</th>
<th>La</th>
<th>PDA</th>
<th>EOT [nm]</th>
<th>$V_{FB}$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>10%</td>
<td>X</td>
<td>700°C, NH$_3$</td>
<td>0.89</td>
<td>-0.58</td>
</tr>
<tr>
<td>80%</td>
<td>O</td>
<td></td>
<td>0.95</td>
<td>-0.85</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.02</td>
<td>-0.93</td>
</tr>
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X-ray photoelectron spectroscopy (XPS) analysis shows that LaO/HfO phase segregation/separation occurs after the thermal process (Fig. 1). Electron energy-loss spectroscopy (EELS) analysis confirmed that La accumulates near the high-k/SiO$_2$ interface by the end of the device fabrication process [2].

### III. RESULTS AND DISCUSSION

In the La-doped HfSiO samples with 10% SiO$_x$, $V_{FB}$ and $V_{th}$ are shifted to the negative direction by about 300 mV, which is due to the La-dipole formation as shown in Fig. 2. EELS analysis in Fig. 1 showed that the

![Fig. 1. XPS analysis shows that by incorporating La, LaOx segregation has occurred after high temperature anneal. La piled up near the HfO$_2$/SiO$_2$ interface from the EELS analysis [31].](image)

![Fig. 2. Transistor CV curves for La-doped samples are shifted to negative direction due to La-dipole formation. For the 80% SiO$_x$, EOT was increased due to reduced dielectric constant. Vth for the 80% SiO$_x$ shows lowest. It appears to be due to oxygen vacancy or more strong La-Si dipole formation [30].](image)
La deposited on the high-k layer piled up at the interface between the SiO$_2$ and high-k layer. To modulate $V_{th}$ and $V_{th}$, the location of La is known to be critical, i.e., no $V_{th}$ shift was observed when the La was at the top of the high-k layer [18]. Once the La diffuses down to the interface layer, the La-O-Si configuration is formed resulting in an interface dipole formation by a charge transfer [15, 18].

In the 80% SiO$_2$ samples, the $V_{th}$ is further reduced in spite of an EOT increase due to reduced dielectric constant. The transistor subthreshold slopes ($S_f$) for the control (no La doping) and sample transistors (both have 10% SiO$_2$ HfSiO dielectric) exhibit similar value of 77 mV/dec. However, higher $S_f$ is observed in the 80% SiO$_2$ devices (Fig. 3). This increased subthreshold slope is attributed to the interface states density ($N_{it}$) increase confirmed by the charge pumping measurements (Fig. 4).

For the 10% SiO$_2$ devices, the interface state density decreased slightly after La incorporation. The 10% SiO$_2$ with La doping exhibits slightly reduced carrier mobility in the low and intermediate field regime compared to the control device (Fig. 5) because the dipole field induces additional carrier scattering even though 300 mV of the $V_{th}$ was shifted in the device with La. This excellent low-field mobility cannot be explained by positive charge incorporation. In addition, the interface state densities from the devices incorporating La are even lower than the control samples. Therefore, interface dipole formation from adding La is believed to be the primary cause of the $V_{th}$ and mobility characteristics. Previous reports proposed a dipole-induced band-offset model to explain the $V_{th}$ shift [16, 18, 31]. Various material screening experiments in search of a band-edge solution have indicated that the interface dipole field is related to the electro-negativity of rare-earth metal elements [15, 16]. If this is true, this band-offset model will be proved by the gate leakage behavior. For the 80% SiO$_2$ devices, mobility degraded significantly. The lower $V_{th}$ and carrier mobility (higher $N_{it}$ and $S_f$) for the 80% SiO$_2$ sample appear to be due to positive charges [6].

A previous La-doped HfO$_2$ study reported that the La dipole led to an increase in the effective barrier height for the substrate injection, which resulted in reduced gate leakage currents. In this study, the gate leakage at $V_{ox}=1.2$ V for the La-doped samples was also reduced due to an offset in barrier height (Fig. 6 and 7). However, the gate leakage difference for the different SiO$_2$ content.
temperature instabilities (PBTI) under the same gate overdrive stress conditions, both types of La-doped devices showed smaller $V_{th}$ shifts. At lower $V_{ox}$ (<1.4 V) condition, La-doping can result in less $V_{th}$ shift because of reduced trapping efficiency, as shown Fig. 8 and 9. With increasing stress voltage ($V_{ox}$>1.8 V), however, all devices showed a similar $\Delta V_{th}$. The similar ratio of $Q_{trapped}$ to $Q_{inj}$ indicates that intrinsic charge trapping is similar regardless of La doping and SiO$_2$ concentration, as shown in Fig. 10. At a lower gate stress voltages, $G_{m}$ degradation was similar. With increased gate stress voltage, however, $G_{m}$ in both La-doped samples degraded more, indicating that the interface degradation becomes more significant and time-dependent dielectric breakdown (TDDDB) characteristics may be worsen (See Fig. 11). From the TDDDB test at a higher gate stress as shown in Fig. 12, La-doped samples show shorter time to breakdown, which are attributed to lower interface quality, most probably associated with the presence of

Fig. 6. At $V_{ox}$=+1.2 V, La-doping reduced gate leakage due to an offset of barrier height [30].

Fig. 7. The La-induced dipole formation between the interface and high-k retarded the injected charges [30].

was not significant. If the larger $V_{th}$ shift for the 80% SiO$_2$ was related to the greater dipole formation, the gate leakage would be lower than that of 10% SiO$_2$ samples, which suggest that La doping results in a positive charge as well.

In previous studies of La-doped high-k dielectrics, the high-k dielectric stacks with La showed better PBTI reliabilities [14, 16]. Other studies reported that incorporating La provided better PBTI immunity at lower bias conditions but reliability under high gate stress field conditions became worse [31, 32]. In the positive bias

Fig. 8. At same gate overdrive stress conditions, La-doping showed less $V_{th}$ shift. For the 80% SiO$_2$, lowest $V_{th}$ was observed [30].

Fig. 9. At lower $V_{ox}$ (<1.4 V) condition, La-doping can induce less $V_{th}$ shift because of reduced trapping efficiency. With increasing stress voltage ($V_{ox}$>1.8 V), however, all devices showed similar $V_{th}$ shift [30].
Fig. 10. Similar ratio of $Q_{impd}$ to $Q_{inj}$ indicates that intrinsic charge trapping are similar regardless of La-doping and SiO$_x$ concentration [30].

La-doping can degrade TED characteristics due to more interface degradation at higher voltage stress conditions [31].

La-doped HfSiO samples showed lower $V_{th}$ and $I_{gat}$, which was attributed to the dipole formation at the high-k/SiO$_2$ interface. With increasing SiO$_x$ content, significant mobility degradation was observed, most likely due to additional La-related charges in the interfacial layer. La-doped devices demonstrate better immunity in the PBTI test and low charge trapping efficiency compared to the control HfSiO.

From the results above, the key factor for improving high field reliability is to mitigate the accumulation of La in the bottom interface layer. However, this can increase the nMOSFET $V_{th}$. With a given condition for incorporating La while maintaining a target $V_{th}$, interface engineering to obtain a more robust interface will be a key factor in reliability.

**IV. CONCLUSIONS**

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