Design of a 25 mW 16 frame/s 10-bit Low Power CMOS Image Sensor for Mobile Appliances

Daeyun Kim and Minkyu Song

Abstract—A CMOS Image Sensor (CIS) mounted on mobile appliances requires low power consumption due to limitations of the battery life cycle. In order to reduce the power consumption of CIS, we propose novel power reduction techniques such as a data flip-flop circuit with leakage current elimination and a low power single slope analog-to-digital (A/D) converter with a sleep-mode comparator. Based on 0.13 µm CMOS process, the chip satisfies QVGA resolution (320 × 240 pixels) that the cell pitch is 2.25 µm and the structure is a 4-Tr active pixel sensor. From the experimental results, the performance of the CIS has a 10-b resolution, the operating speed of the CIS is 16 frame/s, and the power dissipation is 25 mW at a 3.3 V(analog)/1.8 V(digital) power supply. When we compare the proposed CIS with conventional ones, the power consumption was reduced by approximately 22% in the sleep mode, and 20% in the active mode.

Index Terms—CIS, leakage current elimination, single slope A/D Converter, sleep mode, active mode

I. INTRODUCTION

Visual information systems such as digital cameras, broadcast equipment, barcode readers, medical devices, and mobile appliances [1-4] are widely used in many industries. Also, the market for products based on visual information is rapidly growing. When visual information systems are implemented, it is necessary to design an image sensor chip that converts analog image signals into digital codes. Among the many kinds of image sensor chips, the CMOS Image sensor (CIS) is becoming popular because of its high quality and low price. In the field of mobile appliances, the market growth of CISs is especially steep. However, the power consumption of CIS devices is increasing due to the development of high quality CISs. It is now a problem to extend the market for CISs, since the battery life cycle of mobile appliances is limited. Many papers have been published on the reduction of power dissipation [5-12]. It has been reported that the average power consumption of a CIS is 80 mW (minimum 30 mW, maximum 175 mW) [5, 6]. A few ultra-low power CISs are being studied; these feature an extreme structure of low power pixels, or a reduction in the number of column ADCs [7-12]. However, for the conventional CISs, image quality degradation can occur due to noise problems.

In this study, a low-power CMOS image sensor (CIS) for mobile appliances is proposed based on 0.13 µm Samsung CMOS technology. The proposed device has a 320 × 240 (QVGA-class, 76,800-pixel) resolution, and a single slope ADC (SS-ADC) arranged along the column of the pixels. We propose a novel power reduction technique to decrease the active power and standby power consumption. In addition, a new correlated double sampling (CDS) circuit is used to reduce fixed pattern noise (FPN), a major cause of image degradation. The paper is organized as follows. In section II, the overall structure of the CIS and circuit design techniques are discussed. Measurement results are described in section III, and the conclusions are given in section IV.
II. DESIGN OF CMOS IMAGE SENSOR

1. Structure of the CMOS Image Sensor

Fig. 1 shows the full block diagram of a CMOS image sensor. A column parallel CIS is composed of pixels, a single slope ADC, and a digital control block. First, the pixel converts input light signals into electric analog signals. In this study, the pixel was implemented using a four transistor cell with an area of 2.25 µm × 2.25 µm. The circuit diagram of the pixel is not discussed here because it is a very well known scheme. The analog signals are converted into digital codes by the ADC. We used the well-known single slope ADC architecture. Finally, the digital codes of the images are memorized in SRAM. SRAM is composed of a six-transistor memory cell, a row decoder, and a column decoder. Since the memory cell is designed using a full custom technique and layout, the read and write access times are much faster than those of the automatic digital synthesis technique. At the block of final data flip flop, all the digital output codes are synchronized by a main clock. The digital codes are then transferred to a monitor or a computer through an interface chip.

2. Design of the Column ADC

Fig. 2 shows a block diagram and timing diagram of the proposed single slope ADC (SS ADC). When an analog input signal is driven, the ramp signal is also increased with the start of the counter. If the ramp signal is the same as the input signal, the comparator is working. Then, the counter stops counting, the digital code of the input signal is obtained, and the A/D conversion process is completed. Since the column ADC is placed in a small column pitch, the MOS transistor must be as small as possible. In this study, the proposed SS-ADC satisfies these requirements with 10 bit resolution and 1024 gray levels. Since there are many pixels, the SS-ADC has errors by process mismatch and parasitic effects. In addition, there are many random characteristics among the pixels. These heterogeneous characteristics have different digital codes even though the same light is driven. This is called pixel fixed pattern noise (PFPN). It is necessary to compensate the errors. Thus, we used the analog CDS circuits. Applying analog CDS circuits is...
one way to compensate the errors [7-9]. The technique for a comparator's offset removal in a serial connection and the design of a high gain amplifier to remove fixed pattern noise has been reported [10].

3. Proposed Power Reduction Techniques

The design of a CIS for mobile appliances should include low power consumption. The major cause of power consumption at the analog block is different from that at the digital block. In this study, power reduction techniques were introduced by considering the characteristics of each block. The most optimized low power CIS for mobile appliances is proposed at the sleep mode and active mode.

3.1 Power Reduction Techniques in the Sleep Mode

Power consumption in the sleep mode must be almost zero except for the circuit with the standby information. Since the main cause of power consumption at the analog blocks is static power, the power of analog blocks in sleep mode can be suppressed by turn off the bias MOS. The majority of power consumption at the digital blocks can be suppressed by blocking the input clock at the time of sleep mode, because the input clock triggers the dynamic power and short-circuit power. As shown in Fig. 3, the drain-source voltage induces a large sub-threshold leakage current (compared to conventional CMOS technologies) because of the development of the process and the reduction of the threshold voltage. Those leakages during the sleep mode significantly increase the power consumption. In general, it is possible to isolate the power supply or increase the threshold voltage to reduce the leakage power [11].

However, those methods have additional problems such as a large transistor size, slow speed, operating voltage instability due to the blocking switch, and the addition of other transistors. Therefore, in this study, a few circuits to reduce the leakage power are proposed for the sleep mode. Fig. 4 shows a proposed technique to reduce the leakage current using drain-induced barrier lowering (DIBL). According to the stacked structure shown in Fig. 4, the circuits have different leakage power consumption. There are two leakage components such as a sub-threshold leakage and a gate leakage. The sub-threshold leakage current mainly depends on drain-source voltage and threshold voltage. The gate leakage currents ($I_{gate}$, $I_{bgate}$) are generated by a direct tunneling through the gate oxide. The leakage currents can be reduced if we design a low drain-source voltage ($V_{DS}$).
structure. Therefore, we can obtain the smallest leakage power using the digital vectors that drive the gate. The smallest low power stacked structure can be selected without additional circuitry. In this study, all of the digital circuits are fully customized with the proposed DIBL. To minimize the leakage power, many methods have been proposed such as stochastic simulation, integer linear programming analysis, and pseudo-Boolean function techniques, depending on the complexity of the system [12]. We propose a minimum leakage vector (MLV) as shown in Fig. 5. After the leakage power consumption was obtained by SPICE simulation for each digital input code, we obtained the graph shown in Fig. 5. In the graph, the maximum leakage vector and the MLV are assigned. The MLV are composed of clk, memory read/write, column/row control and sync input. Thus, the power consumption in the sleep mode can be reduced if the MLV is memorized at the input code. The input signals are created by FPGA, and we set the signals as MLV when the sleep mode of CIS is operating. However, since the conventional flip-flop circuits hold the latched digital signals, there exist some leakage currents. Thus, the flip-flop circuit shown in Fig. 6 is proposed to obtain the minimum leakage power by using an AND gate while the MLV is applied in the sleep mode.

3.2 Power Reduction Techniques in the Active Mode

Two directions are accessible to reduce power consumption in the active mode. The first technique is to reduce the short circuit current at the image sensor block, and the second technique is to reduce power consumption at the comparator block. We propose a power reduction technique at the comparator block with the termination of the power supply. Fig. 7 shows a circuit diagram for both the conventional and the proposed techniques. The conventional comparator which is shown in Fig. 7(a) uses an analog CDS process to eliminate fixed pattern noise. This comparator structure is an inverter type for small area and low power consumption. However, the inverter comparators have the demerits of noise issue and low gain. To overcome the demerits, we use an offset cancellation technique and a cascaded comparator. In this case, the logic threshold voltage of the comparator is memorized at the capacitor by switches sw3 and sw4 when sw3 and sw4 are closed. At this point, a short-circuit current is created since nMOS and pMOS turn on at the same time. This is because the inverter logic threshold voltage cannot be VDD or GND. The induced short circuit currents increase the power consumption significantly. Thus, we propose a circuit to prevent such a phenomenon, as shown in Fig. 7(b). Fig. 8 is the timing diagram of the proposed comparator. Switches (sw5, 6, sw7) are inserted into the
 comparator for power reduction. Due to the sw5, the short-circuit current at the inverter is almost zero, when the analog CDS is operating. In addition, sw6, 7 can replace the bias voltage VP with the supply voltage VDD, after the end of comparator operation. Thus there are no bias currents at the comparator block. Based on SPICE simulation results, the average power consumption of the proposed SS ADC was reduced by about 35% compared to that of the conventional device. With these power reduction techniques and by adjusting the size of the MOS digital blocks, creating a buffer to prevent undesired short circuit currents, and the simplification of clock signal, we reduced the average power consumption of the proposed CIS by about 20%.

III. EXPERIMENTAL RESULTS

1. Layout of the Proposed CIS

Fig. 9 shows the overall layout of the proposed CIS. The image sensor core area was 2 mm × 1.5 mm (3 mm²) and the total chip size was 3 mm × 2.5 mm (7.5 mm²). The CIS was designed for 0.13 µm Samsung CIS technology. The pixel had a four-transistor structure with a low noise Active Pixel Sensor (APS), and the pixel size was very small (2.25 µm × 2.25 µm). The even columns were placed at the left side of the pixels and the odd columns were placed at the right side of the pixels. Thus, the column layout of the circuit was within a 4.5 µm pitch. To prevent fixed pattern noise, all the columns had the same repetitive patterns. The total number of pixels was 320 × 240 to satisfy the resolution of the QVGA. On each side of the pixels, six dummy pixels were placed to keep the uniformity of the outline pixel characteristics.

2. Measured Results

Fig. 10 shows photos of the proposed CIS chip. Fig. 11 shows photos of the testing printed circuit board (PCB) with a chip-on-board (COB). Because the pixel of the image sensor must be exposed to the outside, the COB proceeded on the PCB without a packaging process. In addition, the image sensor chip was mounted on the body tube and the lens was focused on the subject.

Fig. 8. The proposed timing diagram of low power comparator.

Fig. 9. Full layout of the proposed CMOS image sensor.

Fig. 10. Die photo of the proposed CIS.

Fig. 11. Photo for COB and PCB with the CIS chip.
shows a photo of the overall testing environment of the proposed CIS. The environment was composed of a field-programmable gate array (FPGA) board to generate the input clocks and store the CIS output codes, and a testing board with the proposed CIS.

To operate the CIS, multiple clock signals were required with different timings. Thus, the FPGA was used to generate the clock signals. When we changed the timing of the clock signal, we had more accurate characteristics of the proposed CIS. If the CIS receives the clock signals generated from the FPGA, it creates the output signals of the CIS. Then, the output signals are also transferred to FPGA registers to store the CIS output codes. Finally, after these codes are transferred to the computer, the testing image is shown on a computer monitor.

Fig. 13 and 14 show a teddy bear and the gray chart image taken by the proposed CIS, respectively. The following measurements were obtained: the average of PFPN is 0.4% at dark, the average of column fixed pattern noise (CFPN) is 0.12% at dark, and DR is 40 dB.

### IV. CONCLUSIONS

A low power CIS was developed for mobile appliances with QVGA resolution and Samsung 0.13 μm technology. The power consumption of the CIS was reduced by about 22% in the sleep mode, and by about 20% in the active mode, compared to conventional devices. The proposed CIS took 16 frames/s with 25 mW of power consumption at the standard sampling frequency of 25 MS/s. The chip size of the CIS was 3 mm × 2.5 mm (7.5 mm²), and it had a 12.5 KS/s 10-bit SS-ADC to represent 1024 gray levels. The performance of the proposed CMOS image sensor is summarized in Table 1.

**Table 1. Experimental Results for the proposed CIS**

<table>
<thead>
<tr>
<th>PERFORMANCE SUMMARY</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>Samsung 0.13 μm CIS</td>
</tr>
<tr>
<td>Array Format</td>
<td>320 × 240</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>2.25 μm × 2.25 μm</td>
</tr>
<tr>
<td>Pixel FPN</td>
<td>0.4%</td>
</tr>
<tr>
<td>Column FPN</td>
<td>0.12%</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>40 dB</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>16 frame/s</td>
</tr>
<tr>
<td>ADC Resolution</td>
<td>10 bit</td>
</tr>
<tr>
<td>Power Supply</td>
<td>3.3 V(Analog) / 1.8 V(Digital)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>25 mW</td>
</tr>
<tr>
<td>Chip Area</td>
<td>7.5 mm² (3 mm × 2.5 mm)</td>
</tr>
</tbody>
</table>

### ACKNOWLEDGMENTS

This research was supported by Yonsei university Image Frontier Center(IFC), Samsung Electronics Co. Ltd., and the University ITRC support program supervised by the National IT Industry Promotion Agency(NIPA-2011-C1090-1101-0003)
REFERENCES


Daeyun Kim received the B.S. and M.S. degrees in Semiconductor Science from Dongguk University, Korea in 2007 and 2009, respectively. From 2010, he is working toward to obtain Ph.D. degree at Department of Semiconductor Science, Dongguk University, Korea. He is a student member of IEEK. His major interest is design of CMOS Analog-to-Digital Converter and CMOS Image Sensor.

Minkyu Song received the B.S. and M.S., and Ph.D. degree in Electronics Engineering from Seoul National University, Korea in 1986, 1988 and 1993, respectively. From 1993 to 1994, he was a researcher at Asada Lab., VDEC, University of Tokyo, Japan where he worked in the area of low power VLSI design. From 1995 to 1996, he was a researcher in the CMOS Analog Circuit Design Team of Samsung Electronics, Korea. Since 1997, he has been a professor at University of Dongguk, Korea. He is a member of IEEE and IEEK. His major interest is design of CMOS analog circuits, mixed-mode circuits, and low power digital circuits.