Continuous and Accurate PCRAM Current-voltage Model

Chul-Moon Jung, Eun-Sub Lee, and Kyeong-Sik Min

Abstract—In this paper, we propose a new Verilog-A current-voltage model for multi-level-cell PCRAMs. This model can describe the PCRAM operation not only in full SET and RESET states but also in the partial resistance states. And, 3 PCRAM operating regions of SET-RESET, Negative Differential Resistance, and strong-ON are unified into one equation in this model thereby any discontinuity that may introduce a convergence problem cannot be found in the new PCRAM model. The percentage error between the measured data and this model is as small as 7.4% on average compared to 60.1% of the previous piecewise model. The parameter extraction which is embedded in the Verilog-A code can be done automatically.

Index Terms—Phase-change RAMs, Verilog-A model, unified model, multi-level-cell memories, PRAMs, PCRAMs

I. INTRODUCTION

Phase-Change RAM (PCRAM) has been studied for many years due to better scalability than DRAM and FLASH memory thus being considered now as a strong candidate for future memories [1, 2]. Moreover, PCRAM can be used as Multi-Level-Cell (MLC) applications, where we can store more than two bits at one PCRAM cell because their resistance is able to be controlled as a function of the pulse width and amplitude of programming current [2]. To design read and write circuits of MLC PCRAM, an accurate and reliable current-voltage model is needed.

In this paper, we propose a new accurate current-voltage model which can fit well to the measured data not only in full SET and RESET states but also in partial SET and RESET, where the crystal fraction ratio, C_X is in between the full SET (C_X=1) and RESET (C_X=0). And, this model is reliable because one unified equation describes all the operation regions of PCRAM to prevent any numerical discontinuity point that may introduce the convergence problem in the circuit simulation. Comparing this new model to the previous ones, the models in [3-7] have discontinuity points in their current-voltage relationships which happen at the boundaries between different operating regions of PCRAM. This is caused from that the previous models have described the PCRAM operation using 3 different piecewise-linear models that are representing SET-RESET, Negative Differential Resistance (NDR), and ON region, respectively [7]. These piecewise-linear models could make some discontinuity points at their boundaries between different regions. Though a one-piece model without discontinuity was proposed in [8], it could not describe the partial resistance state well particularly when PCRAM changes from SET to RESET unlike our proposed model. And also, it was based on the SPICE macromodel and the step-like smooth blending function [8] which made the model complicated and its parameter extraction difficult. Comparing the SPICE macromodel with the Verilog-A, the Verilog-A model used in this paper is simpler, more portable, and flexible [7, 9], because the SPICE macromodel is based on circuit elements that have many limitations in describing the
complicated non-linear behavior of PCRAMs. For parameter extraction, the automatic and embedded parameter extraction step that cannot be provided in the SPICE macromodels of PCRAMs such as [8] makes the proposed Verilog-A model very useful in practical applications.

II. UNIFIED AND CONTINUOUS CURRENT-VOLTAGE MODEL FOR MULTI-LEVEL-CELL PCRAM

In Fig. 1(a), at the SET-RESET region, PCRAM resistance is changed between the SET and RESET state according to the calculated crystal fraction ratio. The NDR region shows negative differential resistance between the SET-RESET and ON regions. The \( I_{TH} \) and \( V_{TH} \) mean a threshold current and voltage at which the NDR region starts, respectively. At the \((I_X, V_X)\), a PCRAM enters into the ON region.

A new model equation that can describe PCRAM transient behavior of the partial state can be started from the previous model Eq. (1) in [10], where 3 regional equations of SET-RESET, NDR, and ON regions were merged mathematically using the parallel combination equation. However, the previous model Eq. (1) in [10] could not describe well the NDR region, especially for the partial state that is close to the full SET, as shown in Fig. 1(b). This is because the negative differential resistance is shown very little when the partial state is close to the full SET state. On the contrary, if the partial state is close to the full RESET, the negative differential resistance seems very obvious. Hence, to consider both the partial states that are close to the full SET and full RESET, we use the following merging function [11] in this paper.

\[
f = f_1 \times \exp\left(w \cdot \ln\left(\frac{f_2}{f_1}\right)\right) \tag{1}
\]

Here, \( f_1 \) and \( f_2 \) are two regional equations and \( f \) is a merged equation. \( w \) is the weighting variable. If \( w=0 \), \( f \) becomes \( f_1 \) and as \( w \) becomes 1, \( f \) becomes more and more dominated by \( f_2 \). Assume that \( f_1 \) and \( f_2 \) represent the SET-RESET and ON regional equations, respectively. For the partial state that is close to the full SET, \( f_1 \) can move to \( f_2 \) very smoothly with showing very little negative differential resistance, using Eq. (1). For the partial state that is close to the full RESET, \( f_1 \) is abruptly changed to \( f_2 \), showing the large negative resistance. Hence, using Eq. (1), we can describe the partial state more accurately than the previous Eq. (1) in [10].

Using Eq. (1), the exact model equation of PCRAM current versus voltage relationship can be written by Eq. (2).

\[
V_p = \frac{\ln(k_i R_X I_p + 1)}{k_i} \times \exp\left[w \cdot \ln\left(R_{ON} I_p + V_H\right)/\left(\ln(k_i R_X I_p + 1)\right)\right] \tag{2}
\]

where \( w = 1/\left\lfloor 1 + \left(\frac{I_p - I_{TH}}{I_X - I_{TH}}\right)^n\right\rfloor + 1 \) (0 \( \leq w \leq 1\)).

Eq. (2) combines the SET-RESET regional equation and the ON regional equation into one unified equation using an exponential and a logarithmic function as indicated in Eq. (1). Here a transition phenomenon between the SET-RESET and ON region is modeled using a weighting variable that controls a relative portion of each region. Here \( V_p \) and \( I_p \) are a PCRAM voltage and current, respectively. \( R_X, R_{ON}, \) and \( V_{TH} \) are SET-RESET resistance, ON resistance, and a holding voltage, respectively. \( k_i \) is a coefficient of the SET-RESET region and \( w \) means a weighting variable which is calculated between 0 and 1. The value of \( n \) used in this simulation is 9. As \( n \) becomes larger, we can have a sharper transition from the NDR to the ON region. More specifically, the weighting variable, \( w \) is 0 for the SET-RESET, gets closer to 1 for the ON, and in between 0 and 1 for the NDR. If \( w \) is 0, Eq. (2) can be calculated with \( V_p = \ln(k_i R_X I_p + 1)/k_i \). This term can lead to \( I_p \approx V_p / R_X \) when \( k_i \cdot V_p \) is very small and becomes exponential when \( k_i \cdot V_p \) is large. When \( w=1 \), Eq. (2) becomes \( V_p = R_{ON} \cdot I_p + V_H \) which represents the current-voltage relationship at the ON region. Here \( n \) is 9 and \( I_{TH} \) varies according to the \( R_X \). When \( R_X \) is full SET state \( I_{TH} \) is 0. When \( R_X \) is larger than full SET state \( I_{TH} \) becomes 40 \( \mu A \).

\( R_X \) in Eq. (2) is calculated with the crystal fraction ratio, \( C_X \). \( C_X \) varies in between a full crystal state (\( C_X=1 \)) and a full amorphous state (\( C_X=0 \)), as shown in Eq. (3), according to a calculated state variable, \( X \) [8]. The PCRAM resistance changes according to the cell temperature. The state variable, \( X \) means the thermal
energy that is applied to the PCRAM and has the same dimension as temperature.

\[ R_X = R_{SET} + (R_{RESET} - R_{SET}) \cdot (1 - C_X) \]  

\[ C_X = 1 - e^{-x/X} \cdot A(X) = B \cdot e^{-x/X}, \] and \[ X = \int I \cdot R_{on} \, dt \]

where \( C_X \) is the parameter of \( B \) and \( C \) which are extracted using a simple linear fitting method.

Here \( R_{SET} \), \( R_{RESET} \), and \( R_{ON} \) are PCRAM resistance in the full SET state, the full RESET state, and the ON region, respectively. \( A(X) \) has the parameters of \( B \) and \( C \) which are extracted using a simple linear fitting method.

Fig. 1(c) shows a flowchart of the new PCRAM Verilog-A model. First, it extracts the parameters used in Eqs. (2-3) automatically from the measured current-voltage data. And, \( k_1 \) is calculated with the relationship between \( R_X \) and \( V_{TH} \). Secondly, PCRAM voltage and current are calculated with Eqs. (2-3). The \( R_X \) in Eq. (2) is calculated with Eq. (3) using the state variable, \( X \) which represents thermal energy given to PCRAM cell. A state transition diagram for calculating the \( R_X \) is shown in Fig. 1(c). The full RESET and SET state have their resistance as large as the \( R_{RESET} \) and as small as the \( R_{SET} \), respectively. According to the thermal energy given to PCRAM cell, the \( R_X \) can change in between the \( R_{SET} \) and \( R_{RESET} \). If an amount of thermal energy is not enough to change its state fully from a crystal state (\( C_x=1 \)) to an amorphous (\( C_x=0 \)) or vice versa, the PCRAM goes into the partial RESET or SET state in Fig. 1(b). One thing to note is that this new model can support that PCRAM resistance can move directly from the partial SET to the partial RESET or in the reverse way not passing through the full RESET or full SET.

III. COMPARISON BETWEEN THE CONVENTIONAL AND THE NEWLY PROPOSED MODEL

Fig. 2(a) shows comparison between the measured PCRAM data and the conventional piecewise model, where its 3 piecewise linear models describe the 3 operation regions, respectively. Fig. 2(b) shows the proposed unified model which has only one unified equation to prevent any discontinuity point at the boundaries between different regions. If you look at Fig. 2(b), its current-voltage relationship looks continuous through all the regions not showing any discontinuity at the boundaries. Also this Figure shows how the proposed model fits well to the measured data not only at the full SET-RESET states but also the partial states. To see the discontinuity more in detail, the \( dv/di \) is plotted with respect to the PCRAM current in Fig. 3(a), where we can see a discontinuity point happens in the conventional model that is not found in the proposed model. In Fig. 3(b),
Fig. 2. (a) Comparison between the measured data [1] and the conventional piecewise model [7], (b) Comparison between the measured data [1] and the proposed model. Here $I_{TH}$ is 40 $\mu$A and $I_X$ and $V_X$ are 180 $\mu$A and 0.62 V, respectively. $k_1$ in Eq. (2) is $10.4 \times 10^{-6} R_X + 2.93 [1/V]$.

percentage errors between the measured data and the model are shown. Here the error of the conventional model reaches 60.1% on average, whereas that of the proposed is just as small as 7.4% in the entire PCRAM operation region, where the percentage error is calculated with $\frac{|I_{measured} - I_{simulated}|}{I_{measured}} \times 100$.

The crystal fraction ratio, $C_X$ is plotted with respect to the pulse amplitude of programming current in Fig. 4(a). The $C_X$ is calculated with Eq. (3) and it can change between 0 and 1 according to the state variable calculated with Eq. (3). The parameters in Eq. (3) are $B = 3.9621 \times 10^{-12}$ [J] and $C = -3.0574 \times 10^{-14}$ [J], respectively. The $R_{SET}$, $R_{RESET}$, and $R_{ON}$ are 7 k$\Omega$, 200 k$\Omega$, and 0.947 k$\Omega$, respectively. Fig. 4(b) shows PCRAM resistance changes from the RESET to the SET and vice versa according to the crystal fraction ratio. Comparing the PCRAM resistance calculated with this unified model to the measured data, we can see this unified model fits very well to the measured data both in the SET and RESET states in the entire range of pulse amplitude from 0A to 1300 $\mu$A. Fig. 5(b) shows that PCRAM resistance...
changes according to the programming current applied as shown in Fig. 5(a). By the first SET pulse, the PCRAM changes to the full SET state. In the second RESET pulse, it goes to the full RESET state. The third and fourth pulses are for the partial SET and partial RESET, respectively. In Fig. 5(a) and (b), the simulation was done using practical PCRAM read and write circuits from industry using real SPICE MOSFET parameters of a commercial 0.13-μm process technology.

Fig. 6(a) shows a schematic of PCRAM write and read circuits. In writing ‘SET’ to PCRAM, D\textsubscript{IN} and WR become high to turn on N\textsubscript{1} and N\textsubscript{4}. If N\textsubscript{1} and N\textsubscript{4} are on, I\textsubscript{SET} as large as 550 μA can be applied to PCRAM to decrease PCRAM resistance to R\textsubscript{SET} by the current mirror circuit. When we write ‘RESET’ to PCRAM, D\textsubscript{IN} should be low and WR should be high to turn on N\textsubscript{1} and N\textsubscript{3}. At this time, I\textsubscript{RESET} as large as 1300 μA is applied to PCRAM using the other current mirror thus PCRAM resistance is raised up to R\textsubscript{RESET}. When I\textsubscript{RESET} is applied, PCRAM resistance increases dynamically. For reading PCRAM data, first, READ signal should be high and WR signal should be low to turn on N\textsubscript{0} and N\textsubscript{2} and turn off N\textsubscript{1}, N\textsubscript{3}, and N\textsubscript{4}. At this time the small read current, I\textsubscript{READ} as small as 20 μA is applied to PCRAM.

Fig. 6. (a) Schematic of PCRAM write and read circuit, (b) Voltage waveforms of D\textsubscript{IN}, WR, WR\textsubscript{SET}, WR\textsubscript{RESET}, READ, PCRAM current, PCRAM resistance, and D\textsubscript{OUT}.

When this small I\textsubscript{READ} is applied, PCRAM resistance does not change because I\textsubscript{READ} is too small to change the PCRAM resistance. According to PCRAM resistance, a voltage which is associated with the sensing node ‘SEN’
can be higher or lower than $V_{REF}$. The comparator, $C_1$ can decide whether the voltage is higher or lower. After comparing, the sensed data can be stored at the latch or flip-flop that is connected to the comparator output. Here the simulated array size is $32 \times 32$. Fig. 6(b) shows the waveforms of the $D_{IN}$, WR, WR$_{SET}$, WR$_{RESET}$, and READ, And, PCRAM current, PCRAM Resistance, and Dout are also shown in Fig. 6(b). For the circuit simulation, SAMSUNG 0.13-$\mu$m SPICE parameters were used for the MOSFET devices in Fig. 6(a) and the electrical behaviors of PCRAM was described by the proposed Verilog-A model. The mixed simulation of both CMOS and PCRAM was done by Spectre circuit simulator in Cadence.

IV. CONCLUSIONS

In this paper, we proposed the new Verilog-A current-voltage model for MLC PCRAM. This model fits well to the measured data not only in full SET and RESET states but also in the partial SET and RESET which are in between the full SET and full RESET. Moreover, the percentage error of this model that includes both linear and non-linear current-voltage relationships is lower than 7.4\% on average in the entire operation region, compared to 60.1\% of the conventional piecewise one. The SET-RESET, NDR, and ON regions of PCRAM are unified into one equation in this model thereby discontinuity being able to be prevented. The parameter extraction is straightforward and this extraction step is embedded in the Verilog-A code thus it can be done automatically.

ACKNOWLEDGMENTS

This work was financially supported by the SRC/ERC program of MOST/ KOSEF (R11-2005-048-00000-0), the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2011-0026132), the ETRI System Semiconductor Industry Promotion Center, Human Resource Development Project for SoC Convergence, and the Industrial Strategic Technology Development Program funded by the Ministry of Knowledge Economy (MKE, Korea) (10039239, “Development of Power Management System SoC Supporting Multi-Battery-Cells and Multi-Energy-Sources for Smart Phones and Smart Devices”). The CAD tools were supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

Chul-Moon Jung received the B.S degree in Electronic and Computer Engineering from Kookmin University, Seoul, the Republic of Korea, in 2010. He is currently working toward the Master’s degree of Electronic and Computer Engineering at Kookmin University, Seoul, Korea. His research interest includes the circuit design and modeling for resistive RAM and phase change RAM.

Eun-Sub Lee received the B.S degree in Electronic and Computer Engineering from Kookmin University, Seoul, the Republic of Korea, in 2010. He is currently working toward the Master’s degree of Electronic and Computer Engineering at Kookmin University, Seoul, Korea. His current research interest includes the power management IC design.

Kyeong-Sik Min received the B.S. degree in Electronic and Computer Engineering from Korea University, Seoul, Korea, in 1991, and the M.S.E.E. and Ph. D. degrees in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1993 and 1997, respectively. In 1997, he joined Hynix Semiconductor Inc., where he was engaged in the development of low-power and high-speed DRAM circuits. From 2001 to 2002, he was a research associate at University of Tokyo, Tokyo, Japan, where he designed low-leakage memories and logic circuits. In September 2002, he joined the faculty of Kookmin University, Seoul, Korea, where he is currently an Associate Professor in the School of Electrical Engineering. His research interests include low-power VLSI, memory design, and power IC design. Prof. Min is a technical program committee member of Asian Solid-State Circuits Conference (A-SSCC) and Korean Conference on Semiconductors (KCS). He is a member of IEEE, IEICE, and IEEK.