Design Optimization of a Type-I Heterojunction Tunneling Field-Effect Transistor (I-HTFET) for High Performance Logic Technology


Abstract—In this work, a tunneling field-effect transistor (TFET) based on heterojunctions of compound and Group IV semiconductors is introduced and simulated. TFETs based on either silicon or compound semiconductors have been intensively researched due to their merits of robustness against short channel effects (SCEs) and excellent subthreshold swing (SS) characteristics. However, silicon TFETs have the drawback of low on-current and compound ones are difficult to integrate with silicon CMOS circuits. In order to combine the high tunneling efficiency of narrow bandgap material TFETs and the high mobility of III-V TFETs, a Type-I heterojunction tunneling field-effect transistor (I-HTFET) adopting Ge-Al$_x$Ga$_{1-x}$As-Ge system has been optimized by simulation in terms of aluminum (Al) composition. To maximize device performance, we considered a nanowire structure, and it was shown that high performance (HP) logic technology can be achieved by the proposed device. The optimum Al composition turned out to be around 20% (x=0.2).

Index Terms—Tunneling field-effect transistor (TFET), Type-I heterojunction, narrow bandgap material, high mobility, simulation, nanowire, high performance (HP) logic technology

I. INTRODUCTION

Recently, tunneling field-effect transistors (TFETs) are gaining popularity due to their subthreshold swing (SS) and transconductance characteristics outperforming the conventional FETs [1-3]. On the other hand, it has been pointed out that silicon-based TFETs have rather low on-state current ($I_{on}$), which makes it less competitive in high performance (HP) applications. This weakness can be mostly overcome by switching silicon to narrower bandgap material for higher tunneling efficiency at the source side and the channel material to semiconductor of high electron mobility [4-6]. In order to integrate these materials with silicon CMOS circuits, lattice mismatches should be resolved above all. Ge is a good material because of its integratability with silicon (by using a Si$_x$Ge$_{1-x}$ buffer layer) and its small bandgap for improving tunneling efficiency so that it can be used for a source side material. The device active region, Al$_x$Ga$_{1-x}$As can be grown by metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) to obtain a crystalline channel of high mobility. Al$_x$Ga$_{1-x}$As can be grown directly on Ge since their lattice constants are very similar, $5.6533 + 0.0078x$ Å and $5.658$ Å, respectively. There can be three types of
heterojunction structures and the interface of Ge-AlxGa1-xAs forms a straddling one, Type-I, where $E_C(M_1)<E_C(M_2)$, $E_V(M_1)>E_V(M_2)$, and $E_G(M_1)<E_G(M_2)$. $E_C$, $E_V$, and $E_G$ mean conduction band minimum, valence band maximum, and bandgap energy, respectively. Fig. 1 shows an energy band diagram for a Type-I heterojunction. This scheme realizes a TFET device with an enhanced $I_{on}$ and a suppressed off-state current ($I_{off}$). In this work, a comparative study on Type-I heterojunction TFET (I-HTFET) with homojunction TFETs based on various materials and an optimum design for an I-HTFET of Ge-AlxGa1-xAs-Ge system were performed by 3D device simulation to meet the HP requirements predicted by the most recent technology roadmap [7, 8].

II. STRATEGIES IN DEVICE DESIGN

Fig. 2 illustrates a schematic view of the proposed I-HTFET device. Source and drain (S/D) junctions are made from Ge and the vertical channel from AlxGa1-xAs. Table I summarizes the process parameters and critical dimensions of the device.

The channel length, radius of the nanowire, and gate oxide thickness were 50 nm, 10 nm, and 2 nm, sequentially, which were invariantly used while other parameters might be controlled in simulation works. p + source and n + drain were doped with a concentration of $1 \times 10^{20}$ cm$^{-3}$, and the channel was lightly doped with p-type $1 \times 10^{14}$ cm$^{-3}$ to be nearly intrinsic. The primary design parameter was Al composition ($x$) and it was varied from 0 (GaAs) to 0.4 with 0.05 step. A composition higher than 0.4 resulted in severe degradation of $I_{on}$, or equivalently, impermissibly high threshold voltage ($V_{th}$) for HP applications, which was the reason that an upper limit of 0.4 was considered. For higher reliability of device simulation results, multiple mobility models were included, and quantum tunneling and nonlocal band-to-band tunneling (BTBT) models capable of accurate and consistent prediction of BTBT currents without adjusting model parameters were used [9]. Drain currents ($I_D$’s) were normalized by a unit width in all the $I_D-V_{GS}$ curves. For simple conversion, a device width was presumed to be the circumference of a nanowire. $V_{th}$’s were extracted by a constant-current method which is more practical for evaluating HP logic devices compared with other methods. The reference read current was assumed to be $I_{D, ref}=10^{-7}$ A/μm.

III. SIMULATION RESULTS

1. Advantages over Homojunction TFETs

Fig. 3 compares the $I_D-V_{GS}$ curves from homojunction TFETs of which materials are Si, Ge, and GaAs. Also, a simulated transfer curve from a heterojunction TFET having p+ Ge source, Si$_{0.6}$Ge$_{0.4}$ channel, and Si drain in a previous research has been brought to make comparisons with the proposed device [10]. The channels of all the TFETs are intrinsic while S/D have different doping concentrations.

As shown in Table I, p+ and n+ Ge S/D doping...
concentrations was $1 \times 10^{20}$ cm$^{-3}$. However, the devices in the comparison group were made to have different doping concentrations with intent. For Si and Ge TFETs, S/D junctions were doped with p-type $10^{20}$ cm$^{-3}$ and n-type $10^{18}$ cm$^{-3}$, respectively, and for a GaAs TFET, p-type $10^{20}$ cm$^{-3}$ and n-type $10^{19}$ cm$^{-3}$ were doped. Also, the SiGe HTFET had S/D junctions doped with p-type $10^{20}$ cm$^{-3}$ and n-type $10^{17}$ cm$^{-3}$, respectively. For some devices, even a lower doping concentration in either source or drain junction demonstrates a better performance. For this reason, S/D doping concentrations were intentionally controlled for each device to demonstrate its highest $I_{on}/I_{off}$ ratio with invariance in $I_{on}$ by suppressing $I_{off}$ effectively, by which more reliable and fair comparisons among the devices in their best states were made possible. In Fig. 3, Ge TFET shows the highest $I_{on}$ compared with the other homojunctions TFETs. The $E_G$’s of Si, Ge, and GaAs are 1.12 eV, 0.66 eV, and 1.42 eV, in sequence. Since a smaller $E_G$ boosts the BTBT efficiency and the electron mobilities of Ge and Si are $3,900$ cm$^2$/V·s and $1,400$ cm$^2$/V·s (upper limits), respectively, $I_{on}$ of a Ge TFET is much higher than that of a Si device. On the other hand, there is little difference between the performances of Si and GaAs TFETs. Although GaAs has a much higher electron mobility, $8,000$ cm$^2$/V·s, than Si, $I_{on}$ of a GaAs TFET is more or less the same with that of a Si device since the larger $E_G$ of GaAs substantially degrades the BTBT probability. SiGe is also gaining much popularity as a channel material for HTFET devices [10, 11]. Ge source for higher tunneling efficiency and Si drain for suppressing $I_{off}$ more effectively can be grafted to improve the device performances [10]. In that case, $I_{on}$ converges to that of Ge TFET while $I_{off}$ is kept as low as that of Si TFET as shown in Fig. 3, which is the best performance achievable by the group-IV semiconductor materials. The proposed device with Ge-AlGaAs-Ge heterojunctions shows performances comparable to those of SiGe HTFET. For a good comparison, no Al composition was introduced to match the $E_G$ where the minimum $I_{off}$’s appear. The proposed device shows higher $I_{on}$ and steeper switching. $I_{on}$ is determined by the combinational effect of magnitude of $E_G$ for BTBT at the source-to-channel junction and electron mobility in the channel. One drawback of Ge TFET is high $I_{off}$ as confirmed by Figs. 3 and 4. A smaller $E_G$ of Ge increases the tunneling current by gate-induced drain leakage (GIDL) at the channel-to-drain junction when a negative gate voltage is applied. Fig. 4 shows $I_{on}/V_{GS}$ curves for a Ge TFET and the proposed I-HTFETs based on Ge-Al$_x$Ga$_{1-x}$As system for $x=0, 0.15$, and 0.3, where the Ge-GaAs I-HTFET shows the even higher $I_{on}$. The current drivability is degraded as $x$ increases. For $x=0.15$, $I_{on}$’s of a Ge TFET and a Ge-Al$_x$Ga$_{1-x}$As-Ge I-HTFET are comparable but $I_{off}$ of the latter is much lower, only a few fA/µm. By introducing more Al atoms, $E_G$ gets larger, which is strategic for suppressing $I_{off}$ but on the other hand, the electron mobility is degraded, which lowers $I_{on}$. It is known that the electron mobility is monotonically decreased up to $x=0.45$ [12, 13].

Fig. 5 demonstrates the simulation results for energy band diagrams inside a GaAs TFET and an I-HTFET at a standby mode ($V_{GS}, V_{DS}$)=(0 V, 1 V) and an operating mode, $V_{GS}=V_{DS}=1$ V. p$^+$ Ge source effectively tapers the width of the tunneling barrier at the source-to-channel junction as shown in the right figure. Also, the left...
figure reveals that the effective distance between $E_C$ of n$^+$ drain region and $E_V$ of the intrinsic channel becomes larger for the I-HTFET. This bandgap engineering effectively lowers the BTBT probability for the valence electrons into the n$^+$ drain region, which prominently suppresses $I_{off}$ as previously shown in Fig. 4. Consequently, the analysis results support that introducing a heterojunction formed by Ge and Al$_x$Ga$_{1-x}$As enables to expect improved $I_on$ by higher BTBT probability due to a small $E_G$ of the source-side Ge and high electron mobility of Al$_x$Ga$_{1-x}$As channel while keeping $I_{off}$ sufficiently low by a large $E_G$ of Al$_x$Ga$_{1-x}$As which reduces GIDL at the same time.

2. Design Optimization of the Nanowire I-HTFET

Fig. 6 demonstrates the $I_D-V_{GS}$ curves for I-HTFETs with different Al compositions with $V_{DS}=V_{DD}=1.0$ V. $I_{on}=I_D@V_{DS}=V_{DD}=1.0$ V is degraded as the Al composition increases. $I_{off}$'s are invariant with $x$ values, but as $x$ increases the voltage window for inhibiting the BTBT leakage, GIDL, is widened from 0.1 V for $x=0$ to a value larger than 0.8 V for $x=0.4$. Only for $x=0$ and 0.05, GIDL currents were observed below $V_{GS}=-0.5$ V. Fig. 7 depicts SS as a function of Al composition. An SS has been extracted at a $V_{GS}$ where d$(\log I_D)/dV_{GS}$ has a local maximum out of the $V_{GS}$ region where a device is completely turned off and shows current fluctuations. By adopting this method, the extracted SS values were made the smallest that the devices might have. It was already shown that the proposed I-HTFETs had better SS characteristics than those of Si, Ge, and GaAs homojunction TFETs in Figs. 3 and 4. The obtained SS values in Fig. 7 were below 20 mV/dec and decreased monotonically up to an Al composition of 0.25, where a local minimum was observed. Although the SS characteristics were drastically degraded at $x=0.4$, it was still a very low value. Fig. 8 plots $V_{th}$ as a function of Al composition. $V_{th}$'s were extracted at a reference current of $I_{D,ref}=10^{-7}$ A/μm as mentioned previously. The most recent technology roadmap is suggesting that the $V_{th}$'s be near 200 mV for ultra-thin body (UTB) fully depleted (FD) channel devices aiming HP technologies within...
next five years. The UTB FD device is the category where the proposed I-HTFET device falls into most properly among various types of devices that the roadmap presents. Mapping the $V_{th}$ onto the Al composition through the $V_{th}$-curve in Fig. 8 reveals that the permissible $x$ values should be limited between 0.2 and 0.3. Fig. 9 shows the $I_{on}$ and $I_{off}$ curves as a function of Al composition drawn with open and rigid circles, respectively. The upper left box indicates the minimum $I_{on}$ required for HP applications, which is 1200 $\mu$A/µm by the prediction. 25% is the upper limit in Al composition for the requirement. At the same time, the lower right box indicates the boundary of permissible $I_{off}$ which is defined as $I_D$ at $(V_{GS}, V_{DS})=(0$ V, 1 V), an off-state current at a standby mode. The specified upper limit is 100 nA/µm, which accordingly sets a lower limit in Al composition to be 12%. Finally, The dotted box defines the range of permissible Al compositions, $0.12\leq x\leq 0.25$. Judging from the results made so far on the fundamental direct current (DC) parameters, SS, $V_{th}$, $I_{on}$, and $I_{off}$, it is concluded that the optimum Al composition needs to be around 20%.

IV. CONCLUSIONS

In this work, a Type-I (straddling) heterojunction nanowire tunneling field-effect transistor (I-HTFET) with a channel length of 50 nm based on Ge-Al$_x$Ga$_{1-x}$As-Ge structure has been proposed and simulated for an optimized device design with Al composition as a design variable. The optimum value was found to be around $x=0.2$ in terms of the primary device parameters for HP logic technologies. Due to its silicon-compatibility and capability of achieving high current drivability, extremely low leakage, and excellent swing characteristics, the proposed I-HTFET is believed to be a promising candidate device for the advanced CMOS integrated circuits.

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REFERENCES


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