A 90-nm CMOS 144 GHz Injection Locked Frequency Divider with Inductive Feedback

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Abstract—This paper presents a 144 GHz divide-by-2 injection locked frequency divider (ILFD) with inductive feedback developed in a commercial 90-nm Si RFCMOS technology. It was demonstrated that division-by-2 operation is achieved with input power down to -12 dBm, with measured locking range of 0.96 GHz (144.18 – 145.14 GHz) at input power of -3 dBm. To the authors’ best knowledge, this is the highest operation frequency for ILFD based on a 90-nm CMOS technology. From supply voltage of 1.8 V, the circuit draws 5.7 mA including both core and buffer. The fabricated chip occupies 0.54 mm × 0.69 mm including the DC and RF pads.

Index Terms—Frequency divider, injection locked frequency divider, inductive feedback, LC oscillator, RF CMOS, THz

I. INTRODUCTION

The frequency band beyond 100 GHz, roughly located at the lower end of the THz frequency band (0.1 THz – 10 THz), has been applied to various fields such as imaging, remote sensing, radio astronomy, plasma diagnostics, radar, bio-chemical detection, and so forth. Recently, this band is attracting increasing attention for wireless communication application as the demand for high speed data communication keeps increasing. The frequency band beyond 100 GHz is expected to provide ample bandwidth that will result in increased channel capacity and, hence, increased data transfer rate [1-3]. This paper concerns the issues related to applying such high frequency to the implementation of high-speed commercial wireless communication systems.

In the high frequency communication systems, phase-locked loops (PLLs) are widely employed to provide a stable LO signal [4-5]. For high frequency PLLs, the frequency divider (FD) is considered as a key component along with the voltage-controlled oscillator (VCO). Especially for the first stage of the FD chain, high frequency operation of FD is critically required as it directly receives the signal out of the VCO. For such applications, injection locked frequency dividers (ILFDs) are recently considered as a favored solution as they provide high frequency operation with small DC power dissipation.

In addition to the high performance, cost is also an important factor especially when commercial application is considered. Owing to the rapid progress of nano-scale Si process technologies, Si CMOS technology has been successfully adopted for millimeter-wave applications such as 60 GHz and 77 GHz systems, and now begins to be considered for applications with the frequency band beyond 100 GHz.

This paper presents a study attempting to apply low-cost 90-nm CMOS technology to frequency dividers operating beyond 100 GHz. Noting the fact that most of recent CMOS-based circuits for 100+ GHz frequency bands adopt more advanced but apparently more costly 65 nm (or even more scaled) CMOS technology, this work can be considered as an effort for more production-friendly implementation of such high
frequency circuits. Also, the frequency band near 140 GHz is selected for the operation frequency since this band is favored for wireless applications as the attenuation in the Earth atmosphere shows a minimum around this frequency.

This paper is organized as follows. The basics of various types of FDs are introduced and compared in Section II, and the details of the circuit design for the proposed FD are presented in Section III. In Section IV, measurement results are presented along with measurement environments. Finally, conclusions are drawn in Section V.

II. TYPES OF FREQUENCY DIVIDERS

Frequency division of a periodic signal can be achieved in several different ways. It is general to categorize the frequency dividers into three types; static FD, dynamic (Miller) FD, and injection locked frequency divider (ILFD). The static FDs are based on an edge-triggered flip-flop that is composed of two latches. Differentially driven by the input clock, the two latches provide quadrature output signals at half of the input frequency, resulting in the frequency division. The dynamic FD is based on a feedback loop that incorporates a mixer and a low-pass filter (LPF). The output of the LPF is fed back to the input and then mixed with the input signal, and then fed into the LPF again. This will result in LPF output with half the input frequency leading to the divide-by-2 function, although there are variations in the operation details [6]. Finally, the ILFD is based on an oscillator that is injected by the input signal, the frequency of which is around the integer multiples of the free-running oscillation frequency of the oscillator. The oscillator is then injection-locked to the input and divide-by-integer can be achieved through the locking phenomenon [7].

Traditionally, static FDs and dynamic FDs have been almost exclusively used for practical applications because of its wide locking range. However, their operation frequency is rather limited and will consume prohibitively large DC power when driven to operate at higher frequency bands. ILFD recently emerged as an alternative for mm-wave application due to their high operation frequency with much smaller power consumption. However, their locking range is typically much smaller than those of static and dynamic FDs. Hence, circuit designers face a tradeoff between operating frequency and locking range along with power consumption.

Fig. 1 shows a relation between the operation frequency, locking range, and DC power consumption for recently reported Si-based ILFDs and dynamic FDs that operate at mm-wave bands (static FDs are not included due to lack of sufficient data points at this frequency range) [8-22]. The plot clearly shows the expected tendency: dynamic FDs show wide locking ranges but only at the expense of huge power dissipation, while ILFD can reach higher frequencies with much smaller DC power although the locking range is limited. When power dissipation is considered as a critical design parameter, which is often the case even for high frequency applications as the integration level keeps increasing, ILFDs appear to be the most practical solution for applications beyond 100 GHz.

ILFDs can be sub-categorized into two classes based on the types of the oscillator employed: ring oscillator (RO)-based ILFD and LC-based ILFD. The RO-based ILFD is basically a ring oscillator composed of \( N \) inverter stages that oscillates at the frequency of \( 1/(2N\cdot T_D) \), where \( T_D \) is the time delay of a single inverter stage [23]. Since the phase difference between adjacent stages is \( \pi(1+1/N) \) with the free-running oscillation, the injection of input signal with frequency

![Fig. 1. Reported operation frequency range of various Si-based frequency dividers [8-22].](image-url)
of \(1/(2 \cdot T_D)\) at the same location for each stage will result in the divide-by-\(N\) function. RO-based ILFDs are generally known for its compact size and (potentially) wide locking range due to its low Q-factor, while its operation frequency is rather limited and power dissipation is large compared to LC-based ILFDs [24].

The LC-based ILFD is basically an LC cross-coupled oscillator with an injection node for input signal. The cross-coupled transistor pair results in the negative resistance that compensates for the resistance of the LC resonator tank, satisfying the oscillation conditions. When a periodic input signal is injected at the common mode point of the resonator, the input signal can lock the resonant frequency with a specific division ratio, resulting in a FD function. LC-based ILFDs are currently the most widely accepted ILFD mainly due to their high operation frequency with small power dissipation, although the employed on-chip inductor tends to increase the circuit area.

### III. Circuit Design

The LC-based ILFD was selected for this work as its FD type appreciating its high operation frequency with reasonable power consumption. As mentioned earlier, the narrow locking range is the major obstacle for the practical application of LC-based ILFDs and it needs to be properly addressed. Near the upper boundary of operation frequency, achieving locking operation itself is quite challenging and also closely related to obtaining a wide locking range. Therefore, efforts for improving locking range will lead to higher chances to achieve division function for FDs operating at very high frequency. Hence, an effort is made in this work to generally increase the locking range, which would enable the FD functionality near its operation frequency limit.

There have been various approaches to enhance the locking range in mm-wave and THz range [10, 13, 25-30]. In this work, the inductive feedback is employed to improve the locking range of LC-based ILFDs. The locking range is generally proportional to the RF power of the injected input signal delivered to the core oscillator. The locking range of an ILFD can be expressed as [31]:

\[
\frac{\Delta \omega}{\omega_0} \approx \frac{1}{Q} \cdot \frac{I_{inj}}{I_{osc}}
\]

where \(\Delta \omega\) is the locking range, \(Q\) is the quality factor of the resonator, \(I_{inj}\) and \(I_{osc}\) are the current injected to the tank and the current produced by the oscillating core, respectively. To increase the locking range, therefore, the ratio between \(I_{inj}\) and \(I_{osc}\) in Eq. (1) needs to be increased. The proposed inductive feedback technique is designed to improve the injection efficiency at the injection node, leading to an increase in \(I_{inj}\) delivered to the oscillator core.

Fig. 2 shows the core of the proposed LC-based ILFD together with the conventional LC-based ILFD for comparison. For the proposed circuit, the input signal is injected through the gate of the tail transistor \(M_{in}\). In this configuration, the injection efficiency is given as a gain from the node A to node B in Fig. 2. Hence, the gain needs to be improved for increased locking range. This gain of the input stage is necessarily compensated by the parasitic capacitance \(C_{gd}\). In the proposed technique in this work, a feedback inductor \(L_f\) is inserted between the gate and drain of \(M_{in}\), partially resonating out this capacitance and thus improving the injection efficiency. This will lead to improved injection efficiency and eventually to increased chance for frequency division functionality of the ILFD at higher frequencies. It is noted that the addition of the feedback inductor will lead to a finite increase in loss besides the capacitance cancellation if the Q-factor of the inductance is not sufficiently high. A detailed analysis of
the effect of the inductive feedback and resultant performance improvement can be found in [32]. The schematic of the completed ILFD is shown in Fig. 3 along with the device dimensions. The unit finger width was chosen as 1.5 mm, which was roughly the optimum for the highest operation speed.

IV. MEASUREMENT RESULTS

The LC-based ILFD was fabricated in TSMC 90-nm 1P9M CMOS technology. The chip photo of the fabricated circuit is shown in Fig. 4. The chip size is 0.54 mm × 0.69 mm. Testing circuits at D-band is not trivial, and the ILFD measurement employed in this work is described below in rather detail, which is fully based on on-wafer probing.

The block diagram of the measurement environment is illustrated in Fig. 5. The input signal generated from an Agilent E8257D is up-converted to D-band by a Quinstar frequency tripler, and then injected to DUT through WR-6 waveguide parts and a GGB D-band GSG waveguide probe. The output signal from the FD, which is around 70 GHz range, is probed by a cable-based GGB GSGSG probe and down-converted by an Agilent 11974 V-band preselected mixer, and then measured by an Agilent 4407B spectrum analyzer. It is noted that one port of the GSGSG probe is 50 Ω-terminated since the FD output is differential while the measurement is single-ended. The RF power of the injection signal is measured at the output of the tripler with Erickson PM4 power meter, and the loss through the waveguide parts and the probe was extracted from a separate loss measurement and then used for final calibration. Output signal displayed by the spectrum analyzer was used for the state decision of the locking.

The measured free-running output spectrum of the fabricated ILFD was 72.385 GHz as shown in Fig. 6(a), which is reasonably close to the simulated value of 71.1 GHz. Fig. 6(b) shows the output spectrum of the circuit at the presence of input signal injection at 144.6 GHz, which clearly shows a locking behavior as indicated by significantly improved phase noise and output power compared to the free-running state. For the estimation of the locking range, the input sensitivity curve was created from the measurement as depicted in Fig. 7. DC bias current used for the measurement including both core and buffer was 5.7 mA with $V_{DD}$ and $V_{BUFF}$ of 1.8 V, leading to DC power consumption of 10.2 mW. The measurement shows that the frequency dividing is indeed achieved with input power down to -12 dBm, and the measured locking range is 0.96 GHz (144.18 – 145.14 GHz) at -3 dBm of input power. Note that the locking range is expected to be larger if the input power is increased up to 0 dBm, which is the standard value for ILFD measurement. The measured locking range shows a fairly good agreement with the simulated value of
The measured performance of the LC-based ILFD is compared with previously published results from CMOS-based ILFDs in Table 1. Fig. 8 locates the data point of the present work in the operation frequency vs. locking range space along with data points from prior arts. It clearly shows that the proposed ILFD in this work exhibits the highest operation frequency for 90-nm CMOS technology, extending the performance envelope of the relatively low-cost technology. Although the locking range is rather narrow, it is expected to be improved with further optimization of the size of the feedback inductance as well as the active device dimension.

### V. CONCLUSIONS

In this paper, a 144 GHz ILFD employing the inductive feedback has been developed in a 90-nm Si RFCMOS technology. It is demonstrated that divide-by-
2 operation is achieved with input power down to -12 dBm, with measured locking range of 0.96 GHz (144.18 – 145.14 GHz) at input power of -3 dBm. This is the highest operation frequency for ILFD with 90-nm CMOS technology reported so far. The locking range is expected to be improved with further optimization of the circuit. This work indicates that Si-based low-cost technology can be readily applied to frequency band well beyond 100 GHz, bringing Si-based THz integrated systems closer to the reality.

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