A CMOS Frequency divider for 2.4/5GHz WLAN Applications with a Simplified Structure


Abstract—In this paper, a dual-band integer-N frequency divider is proposed for 2.4/5.2 GHz multi-standard wireless local area networks. It consists of a multi-modulus imbalance phase switching prescaler and two all-stage programmable counters. It is able to provide dual-band operation with high resolution while maintaining a low power consumption. This frequency divider is integrated with a 5 GHz VCO for multi-standard applications. Measurement results show that the VCO with frequency divider can work at 5.2 GHz with a total power consumption of 22 mW.

Index Terms—Frequency divider, frequency synthesizer, phases switching, wireless local area network (WLAN)

I. INTRODUCTION

The wireless communication industry is currently experiencing a tremendous growth. For Wireless LAN applications, the IEEE 802.11 multiple standards have been widely adopted for the short-range communication [1, 2]. The frequency synthesizer, which is usually formed by a Phase-Locked Loop (PLL), is a major and critical component of a wireless transceiver because it operates at high frequency and consumes a large portion of the total power in the transceiver. Currently, there exist several different standards of operation, for example, the 2.4 GHz 802.11 b/g and 5.2 GHz 802.11a/ HIPERLAN-2 networks; and thus a multi-standard frequency synthesizer is desirable for operations under different wireless systems. Numerous research efforts have been carried out on multi-band multi-standard receivers [3-9]. The performance in power consumption and channel selection of a frequency synthesizer are limited by the two important building blocks, namely the frequency divider and voltage-controlled oscillator (VCO). The fractional-N frequency synthesizer has been used to achieve high resolution [2]. However, it has problem of spurs and a complex circuit, e.g. the sigma-delta modulator is needed to suppress spurs [2, 10]. On the other hand, the integer-N frequency synthesizer takes the advantage of low-cost and low-spur sideband performance [10]. The frequency divider in the integer-N frequency synthesizer is usually formed by a prescaler, a program counter (P counter) and a swallow counter (S counter) [11] which can provide a programmable division ratio of \( N \times P + S \), where \( N, P \) and \( S \) are the division ratios of the prescaler, \( P \) counter and \( S \) counter, respectively. In the conventional designs [1], dual-loop or triple loop frequency synthesizers, additional mixers are used to obtain desired frequencies. This requires complex topologies and introduces additional power consumptions. In this paper, a wide-band high-resolution programmable frequency divider with a simple topology is proposed. This paper is organized as follows. In section II, the design considerations for the frequency synthesizer are reviewed. Section III describes the structure and operation of the proposed circuits. The experimental results are summarized in section IV. Finally, the conclusions are given in Section V.
II. Design Considerations

The considerations in the frequency synthesizers design include: high operating frequency, low power consumption, and low phase noise. High operation frequency and low power consumption are key considerations in the frequency divider design. Injection locked frequency divider has been proposed to achieve high operation frequency and low power consumption [10]. However, it is with limited bandwidth and hard to achieve variable division ratios [10]. Therefore, in the applications of multi-channel WLANs, the digital frequency divider is commonly used. The operating frequency of digital frequency divider is inversely proportional to the propagation delay while digital building blocks in high frequencies take major contribution to the total power consumption because the power consumption is usually linearly proportional to the operating frequency. In the multi-standard applications, there are some additional considerations: as the frequency synthesizer is used for multiple standards, all the carrier frequencies of these standards must be produced. The VCO and the frequency divider must be adapted to provide the desired frequencies for down-conversion and up-conversion in the transceiver. The major challenge lies in the frequency divider design, which must provide a wide range and a high resolution for the frequency divisions. To save area and power consumption, a simple topology is preferred.

III. Circuit Implementations

A simple method to achieve the 2.4/5.2 GHz dual-band operation can be realized by utilizing a 5 GHz oscillator for the 5.2 GHz wireless LAN and a divide-by-2 unit to provide 2.4 GHz frequency band. With this method most of the circuits for dual-band operation can be shared. Considering the gap between the oscillator (2.6 GHz) of the divide-by-2 and the 2.4 GHz wireless LAN applications, a wide operating range is required for both the oscillator and the frequency divider.

1. Wide band Voltage-Controlled Oscillator

The voltage controlled oscillator (VCO) is a key building block in the design of a frequency synthesizer.

Fig. 1. The topology of the proposed VCO.

The complementary cross-coupled structure which is suitable for high frequencies of oscillation is used, as shown in Fig. 1.

It utilizes NMOS and PMOS cross-coupled amplifiers as the negative resistance to compensate for the losses in the LC tank. The resonant tank includes the parasitic capacitances of MOS transistors and of the inductor. Frequency tuning is realized by control of back gate voltages of the varactors. Two groups of varactors, which are implemented with PN varactor, are controlled with two external DC voltage sources, namely Band and $V_{\text{CONT}}$. The size of the varactors is 100 fF. The tuning range of the VCO is around 15%, from 4.7 GHz to 5.3 GHz. Larger varactors could be used to achieve a wider tuning range by adjusting the transistor size accordingly. In the operating range of 5 GHz, the performance of phase noise is mainly determined by the quality factor of the inductor. The size of the inductor is carefully optimized to obtain a higher quality factor.

2. Dual-band frequency divider

A high resolution is required to cover all the center frequencies of multi-standards applications, as the frequency synthesizer is based on the integer-$N$.

This demands a low-power and high-resolution frequency divider. The most challenging block in the design of a high frequency programmable divider is the prescaler. In conventional designs [1, 10], a divide-by-2 unit is placed before the prescaler, making all the division ratio in the order of 2. The method sets a limitation in the available division ratios. The phase
switching technique, as proposed in [12] can be implemented to solve this problem.

Fig. 2 shows the topology of a phase switching prescaler [12]. The phase switching prescaler has many advantages over the conventional prescaler based on the Johnson cell [12]. The phase switching prescaler can be implemented with only one full speed divide-by-2 unit. However, the conventional prescaler normally utilizes a divide-by-2/3 or 4/5 unit, which has additional power consumption and propagation delay. Moreover, the dual-modulus operation by phase switching makes this topology suitable for large division ratios and multi-band operations. In the conventional design, an end-of-counting detector is employed to detect all divide-by-2 stages’ output. The logic detector becomes complex with the increase of number of the divide-by-2 stages. This creates difficulties in the dual-band operations as the detector is used to detect all stages’ status. For the phase switching prescaler, the change of modulus is controlled by switching between different phases at the ending of a division cycle. Only a 2-to-1 MUX in the divide-by-2 chain is required when changing from divide-by-\(N/N+1\) to divide-by-\(2N/2N+1\). This topology makes it easy to perform dual-band operations.

As shown in Fig. 3, a 2-to-1 MUX is used in the divide-by-2 chain to select different divide-by-2 stage as the output, which is similar to the multi-modulus divider in [13]. To increase the operating frequency, the imbalanced phase switching, which can switch between 25% duty cycle phase signals instead of 50% duty cycle signals, is used [14]. This prescaler can provide dual-band control in additional to the dual-modulus operation. The merit of the proposed design is that, the output of the prescaler is divide-by-\(N/N+1\) and divide-by-\(2N/2N+1\). In the conventional design with a divide-by-2 in the oscillator, the output of the oscillator and divide-by-2 unit are divide-by-\(N/(N+1)\) and divide-by-\(2N/(2N+2)\). The proposed design is able be integrated with the pulse-swallow counters to provide programmable division ratios easily. The total division ratio of the proposed frequency divider will be \(N \times P + S\) and \(2N \times P + S\). In the conventional design, the ratio is \(N \times P + S\) and \(2(N \times P + S)\) which are limited to the multiple of 2.

In a wide-range high-resolution operation, the configuration of the digital counter plays an important role. In an integer-\(N\) frequency synthesizer, the total division ratio is given by \(N \times P + S\). In the conventional design, only the \(S\) counter is partially programmable [10]. If all stages of both \(P\) and \(S\) counters are programmable, the total division ratios available will be increased. To achieve high-resolution, wide-band operation with a low power consumption, the digital counter proposed in the [11] is used in this frequency divider.

**IV. EXPERIMENTAL RESULTS**

The proposed circuits are fabricated using the Chartered Semiconductor Manufacturing (CSM) 0.18 \(\mu\)m 1P6M CMOS process. Measurement is carried out on wafer by using a Cascade probe station. The output of the VCO is measured by Agilent 26.5 GHz spectrum analyzer. In the VCO’s test chip, common-source buffers with 50 ohm resistive loads are used. Due to parasitic capacitors in the NMOS of the buffers, the output frequency reduces slightly. Fig. 4 shows the output spectrum of the VCO, and its operating range is summarized in Fig. 5. The phase noise of the VCO at 5GHz is presented in Fig. 6. At the offset of 1MHz, the phase noise is about -105 dBC/Hz.

The dual-band prescaler and the frequency divider are integrated with the frequency divider combining with the VCO. Post-layout simulation results show the prescaler implemented with the proposed 2-to-1 phase switching technique is able to work at a input frequency of 5.2 GHz.
proposed measurements, a transgate and an inverter are placed in the input signal for measurement. The mismatch caused by the input slightly reduces the operating frequency.

The prescaler is implemented with the Giga-Hertz range digital counter [11] to realize a wide range high resolution frequency divider. The single-ended input source is provided by the Anristu 68347C 10 MHz-20 GHz signal generator. The output signals are captured by Lecroy Wavemaster 8600A 6G oscilloscope. The standalone frequency divider can operate at an input frequency of 4.5 GHz. Fig. 7 shows the output waveform of the prescaler at an input frequency of 4 GHz having dual-modulus and dual-band operation. Fig. 8 shows the operating frequency vs. power consumption for the proposed frequency divider which is implemented with this prescaler and two counters in [11]. Here the division ratio of the proposed frequency divider is set as 1171 to demonstrate the programmable division ratio. The covering of different WLAN standards can be achieved by changing the configuration of N, P and S. The power consumptions for the VCO and frequency divider are 7 mW and 15 mW, respectively. Fig. 9 shows the die photo of the proposed VCO with dual-band frequency divider.
Function blocks including VCO, prescaler and counter are marked in the figure. Table 1 presents the result from this work and those from other dividers in references in terms of power consumption, operating frequency, availability of the division ratios and F.O.M. F.O.M. is defined as operating frequency times bandwidth over power consumption.

V. CONCLUSIONS

In this paper, a multi-standard WLAN frequency synthesizer is proposed, including a VCO with a wide tuning range, a dual-band dual-modulus phase switching prescaler and Giga Hz range digital counters. The VCO and frequency divider is able to cover the application of 5.2/2.4 GHz wireless LAN operations with low power consumption. The performance of the VCO and the frequency divider are verified with a CMOS technology.

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REFERENCES


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