Avalanche Hot Source Method for Separated Extraction of Parasitic Source and Drain Resistances in Single Metal-Oxide-Semiconductor Field Effect Transistors

Seok Cheon Baek, Hagyoul Bae, Dae Hwan Kim, and Dong Myong Kim

Abstract—Separate extraction of source \( (R_S) \) and drain \( (R_D) \) resistances caused by process, layout variations and long term degradation is very important in modeling and characterization of MOSFETs. In this work, we propose “Avalanche Hot-Source Method (AHSM)” for simple separated extraction of \( R_S \) and \( R_D \) in a single device. In AHSM, the high field region near the drain works as a new source for abundant carriers governing the current-voltage relationship in the MOSFET at high drain bias. We applied AHSM to n-channel MOSFETs as single-finger type with different channel width/length \( (W/L) \) combinations and verified its usefulness in the extraction of \( R_S \) and \( R_D \). We also confirmed that there is a negligible drift in the threshold voltage \( (V_T) \) and the subthreshold slope \( (SSW) \) even after application of the method to devices under practical conditions.

Index Terms—MOSFET, source resistance, drain resistance, hot-carrier, parameter extraction, parasitic resistance, avalanche multiplication

I. INTRODUCTION

Scaling down of MOSFETs (Metal-Oxide-Semiconductor field effect transistors) in CMOS (complementary MOS)-based technology is a primary approach for faster operation and higher integration [1, 2]. Accurate modeling and extraction of characteristic model parameters in MOSFETs, especially parasitic source and drain resistances \( (R_S \) and \( R_D) \), are crucial to the simulation and implementation of power devices, high performance CMOS devices, and their integrated circuits. With fast scaling down of the device, the total parasitic resistance \( (R_{SD}=R_S+R_D) \) is getting comparable to the channel resistance \( (R_{Ch}) \) controlled by the gate voltage [3]. In high frequency and high speed CMOS systems with scaling down of MOSFETs, \( R_S \) and \( R_D \) play an important role in long term performance degradation and reliability of integrated systems. However, effects of \( R_S \) and \( R_D \) are different from each other in MOSFETs and integrated circuits [4]. It is well known that the electrical performance and reliability parameters, including transconductance \( (g_m) \), saturated drain current \( (I_{D, sat}) \), cut-off frequency and noise figure, depend more on \( R_S \) than on \( R_D \) [5, 6]. However, due to the difficulty on the separated extraction of \( R_S \) and \( R_D \) in MOSFETs without conductive DC gate current through the insulated gate, parasitic resistances are, generally, assumed to be \( R_S=R_D=R_{SD}/2 \) regardless of the possible asymmetry in practical MOSFETs. Although several novel methods have been proposed to resolve those issues, those methods are highly complicated or require more than one device or additional patterns for a separated extraction of \( R_S \) and \( R_D \) [7-15].

In this work, considering asymmetries caused by an intentional and/or accidental layout, process variation, device size and long term degradation, we propose the “Avalanche Hot Source Method (AHSM)” for separated extraction of \( R_S \) and \( R_D \) in a single MOSFET. In AHSM, the high field region near the drain works as a “hot
source” for carriers due to the avalanche multiplication process and the current-voltage relationship is limited by the $R_D$ at high drain bias [16, 17]. We applied the proposed method to n-channel MOSFETs with different channel width/length ($W/L$) combinations and verified its usefulness in robust extraction of $R_S$ and $R_D$.

II. AVALANCHE HOT SOURCE METHOD FOR SEPARATED EXTRACTION OF RS AND RD IN MOSFETS

Carriers flowing in n-channel MOSFETs under avalanche multiplication at large drain bias $(V_{DS})$ are schematically shown in Fig. 1 including $R_S$ (source resistance), $R_D$ (drain resistance), $R_G$ (gate resistance) and $R_B$ (substrate resistance). The component ① describes channel electrons moving from the source to the drain in n-channel MOSFETs at the gate voltage $(V_{GS})$ greater than the threshold voltage $(V_T)$. Components ②–⑤ are for electron-hole pairs (EHPs) generated by the impact ionization of hot carriers in the high field region near the drain at a large $V_{DS}$. Component ② is for lucky hot electrons injected into the gate oxide by the vertical field and ③ for electrons drifted to the drain by the lateral field after impact ionization. Components ④ and ⑤ are for moving holes after EHP generation by impact ionization due to hot electrons in the channel. The component ③ is for electrons collected to the drain in the high field region close to the drain. In AHSM for separated extraction of $R_S$ and $R_D$ in MOSFETs, we focus on the current component ③ at large drain bias in MOSFETs for characterization [18, 19].

Meanwhile, in the saturation mode of MOSFETs under a large $V_{DS}$ ($V_{DSat}<V_{DS}<V_{Do}$) without avalanche multiplication by hot channel carriers, the normal saturated drain current ($I_{DSat}$) with a channel length modulation ($\lambda$) is described by

$$
I_{DSat} \approx \mu_{eff} C_{ox} \frac{W}{L} (V_{gs} - V_T - I_{DSat} R_G) \left[ 1 + \lambda (V_{gs} - I_{DSat} R_G + R_G) \right]
$$

with $\mu_{eff}$=the effect channel carrier mobility, $C_{ox}$=the oxide capacitance per unit area, $\lambda$=the channel length modulation parameter, $V_{sat}$=the saturation velocity of the channel carriers in short channel MOSFETs and $V_{DSat}$=the drain saturation voltage ($V_{DSat}=V_{GSat}$, $V_T$ in long channel and $V_{DSat}=L_{eff} C_{ox} V_T$ in short channel MOSFETs; $\lambda_{sat}$ is the saturation field in the channel). The gate bias-dependent critical drain voltage $V_{Do}$ is defined as the drain voltage at the turn-on of the avalanche multiplication process in MOSFETs. If the drain current is sharply increased by the component ③ due to EHPs generated by hot channel carriers at $V_{DS}>V_{Do}$, the internal drain voltage $V_{DS0}$ is not controlled by $V_{GS}$ or $V_{DS}$ as in MOSFETs. The internal drain voltage is defined to be $V_{DS0}=V_{DS-I_D}(R_S+R_D)$ as the real drain-to-source voltage after de-embedding the voltage drop across parasitic $R_S$ and $R_D$. Although the amount of EHP is determined by the inversion charges through the vertical field by $V_{GS}$ and the lateral field by $V_{DS}$, the variation in $V_{DS0}$ is negligible.

Fig. 2 shows the field distribution under a specific bias, the relative amount of EHP and location of effective hot source with this distribution. Fig. 2 clearly tells that the source of the current generated by the component ③ ends up to be close to the drain edge regardless of $\Delta L$ ($\Delta L = L_{eff} (L_{gate} = L_{eff} = \text{effective channel length})$). Therefore, the internal drain voltage and the amount of EHP are limited by the voltage drop across $R_D$. This is because most of the avalanche-generated excess electrons are collected to the drain and causes a voltage drop only across $R_D$. In this case, the drain current $I_D$ and $I_{Do}$ after the turn-on of the avalanche multiplication ($V_{DS0}$) is

![Fig. 1. Schematic illustration of carriers moving in n-channel MOSFET under large drain bias ($V_{Do}$) with parasitic source ($R_S$), drain ($R_D$), gate ($R_G$) and substrate ($R_B$) resistances. The component ③ is for electrons collected to the drain in the high field region close to the drain and this is a main component for AHSM in the separated extraction of $R_S$ and $R_D$ in MOSFETs.](Image)
described by the sum of two current components \((I_{Do})\) and \(I_{D,hot}\), component \((3)\), as schematically shown in Fig. 3(b) as an inset,

\[
I_D = I_{Do} + I_{D,hot}
\]

\[
I_{Do} = I_D \Big|_{V_{Do} \rightarrow V_{Do}} \text{ in Eq. (1)}
\]

\[
I_{D,hot} = qn_{ch}(1 + M)\mu_mW = \frac{(V_{in} - V_{Do})}{R_D} \text{ with avalanche process at } V_{in} > V_{Do}.
\]

Therefore, we finally obtain

\[
I_D = I_{Do} + I_{D,hot} = I_{Do} + \frac{V_{in} - V_{Do}}{R_D} (\text{for } V_{in} > V_{Do})
\]

for the AHSM under large drain bias with \(I_{Do}\)=the normal drain current at \(V_{DS}=V_{Do}\) without the avalanche process, \(M\)=the avalanche multiplication factor and \(n_{ch}=V_{GS}\)-controlled channel carrier concentration.

\(I_{D,hot}\) is defined as the hot-carrier-induced avalanche drain current after the turn-on of the avalanche multiplication process by the impact ionization of hot channel carriers. Due to an abrupt increase of the hot channel carriers, the drain region with the high electric field works as a hot source and the current is limited by the extrinsic drain resistance \(R_D\).

Although the absolute value of the drain current \(I_D=I_{Do}+I_{D,hot}\) depends on the bias condition and the device structure, the slope \((\partial I_D/\partial V_{DS})\) is prominently determined by \(R_D\) because the avalanche-generated carrier-limited drain current \(I_{D,hot}=(V_{DS}-V_{Do})/R_D\) in the hot source region under large bias \(V_{DS} > V_{Do}\). Therefore, it is possible to extract \(R_D\) from the slope of the \(I_D-V_{DS}\) characteristics with a controlled avalanche process at \(V_{DS} > V_{Do}\) using

\[
\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{R_D} \text{(for } V_{DS} > V_{Do})
\]

This is the “Avalanche Hot Source Method” for separated extraction of \(R_D\) from \(R_S\) in \(R_{SD}\) because the high field region near the drain works as a new carrier source/supplier (avalanche hot source) of a large amount of excess EHP’s governing the current-voltage relation in the MOSFET with parasitic resistances under the high field formed by the large drain bias.

III. EXPERIMENTAL RESULTS: SEPARATED EXTRACTION OF RD AND RS

Experimental \(I_D-V_{DS}\) characteristics of the n-channel MOSFET (thickness of the gate oxide: \(t_o=7.3\) nm, gate width/length \(W/L=120\) \(\mu m/0.35\) \(\mu m\) and typical overlap length = 0.045 \(\mu m\) fabricated using a 0.35 \(\mu m\) CMOS process) are shown in Fig. 3. The threshold voltage and the subthreshold slope were measured to be \(V_I=662-668\) mV and \(SSW=81-83.5\) mV/dec, respectively, from MOSFETs with various \(W/L\)-combinations as summarized in Table I. In the \(I_D-V_{DS}\) characteristics for MOSFETs under test, there are four different regions to be categorized: a) Linear region with \(V_{DS} < V_{Dsat}\) b) Saturation region with \(V_{Dsat} < V_{DS} < V_{Do}\) c) Transition region for \(V_{Dsat} < V_{DS} < V_{DDo} \) with an increasing \(I_D\) and d) Avalanche hot source region with a constant slope in the \(I_D-V_{DS}\) characteristics at \(V_{DS} > V_{DDo}\).

In the hot source region under high drain bias \((V_{Do}=5.0-5.7\) V for \(V_{GS}=1.0-1.4\) V), the slope in the \(I_D-V_{DS}\) curve is constant and \(R_D\) is obtained from 1/slope as shown in Fig. 3(b). As expected, the hot source turn-on voltage \(V_{Do}\) depends on \(V_{GS}\) because the carrier density available to the avalanche process for the hot source is increasing with \(V_{GS}\).

Even at a low gate voltage \((V_{GS}=V_I)\), the AHSM gives a relatively accurate \(R_D\). This is because the effective hot source region moves far from the drain with increased charges supplied from the channel, as shown in Fig. 2.
Fig. 3. $I_D$-$V_{DS}$ characteristics of n-channel MOSFET ($t_{ox}=7.3$ nm and $W/L=120$ μm/0.35 μm). (a) Over a wide range of the drain bias $V_{DS}$ (b) The hot source region with avalanche multiplication at large drain bias for AHSM. In the constant slope region, 1/slope$\equiv R_D$ is independent of the gate bias. The equivalent circuit for the MOSFET with the avalanche hot carrier multiplication is schematically shown in Fig. 1.

The gate-bias dependent total resistance $R_{TOT}$ ($R_{TOT}=R_S+R_D+R_{Ch}$ with $R_{Ch}$=channel resistance) obtained from $I_D$-$V_{DS}$ characteristics in the linear region with a small $V_{DS}$ (=0.05 V) is shown in Fig. 4(a) for n-channel MOSFETs with $W=120$ μm and $L=0.35, 0.70$ and 1.05 μm. Therefore, the total source-to-drain resistance $R_{TOT}$ can be obtained from

$$R_{TOT}(V_{GS}) = \frac{V_{DS}}{I_D} + \frac{L_d}{\mu_C W (V_{GS}-V_T)}$$  \hspace{1cm} (7)$$

with $V_{GS}$-independent $R_{SS}=R_S+R_D$, including a $V_{GS}$-dependent channel resistance and channel resistance per unit channel length ($r_{ch}$) [20].

$R_S$ and $R_D$ extracted by the proposed AHSM are shown in Fig. 4(b) for different $W/L$ combinations ($W/L=40/0.35$, 80/0.75, 120/0.35, 120/0.7, 120/1.05 μm/μm) of n-channel MOSFETs. The channel resistance $R_{Ch}$ strongly depends on the gate bias for the MOSFET under characterization. As far as we obtain $R_S$ and $R_D$ from AHSM, $R_{Ch}$ can be obtained from $R_{Ch}=R_{TOT}-(R_S+R_D)$ from the extracted $R_{TOT}$ in the $I_D$-$V_{DS}$ characteristics under the linear mode of operation with a small $V_{DS}$. $R_S$ and $R_D$ obtained by AHSM are extracted to be $R_S=10.1$–23.2 Ω and $R_D=9.9$–23.1 Ω for MOSFETs as summarized in Table 1 for different $W/L$ combinations on the same wafer. We also summarized the normalized value of the resistance as ($R \times W$=12 MΩ cm) for verification of the gate width effect.

In the Table 1, the $R \times W$ for $W=40$ μm is small because the effective channel width ($W_{eq}$) becomes wider with decreasing the gate width. It clearly shows that the AHSM reflects a change depending on the device size. We also note that there is a shift in the ratio of $R_{SS}$ to $R_{TOT}$ when the gate length changes [3] because the channel resistance ($R_{Ch}$) depends on both the gate bias and channel length while $R_S$ and $R_D$ are independent of them. Lastly, we also checked the change of device parameters after 20 times of repeated hot-source

<table>
<thead>
<tr>
<th>$W/L$ [μm/μm]</th>
<th>40/0.35</th>
<th>80/0.35</th>
<th>120/0.35</th>
<th>120/0.7</th>
<th>120/1.05</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_T$ [mV]</td>
<td>668</td>
<td>666</td>
<td>662</td>
<td>664</td>
<td>663</td>
</tr>
<tr>
<td>$</td>
<td>\Delta V_T</td>
<td>$ [mV]</td>
<td>10</td>
<td>10</td>
<td>57</td>
</tr>
<tr>
<td>$SSW$ [mV/dec]</td>
<td>83.5</td>
<td>81</td>
<td>81.4</td>
<td>83.3</td>
<td>82.7</td>
</tr>
<tr>
<td>$ASSW$ [mV/dec]</td>
<td>4.8</td>
<td>3.9</td>
<td>3.9</td>
<td>2.4</td>
<td>1.3</td>
</tr>
<tr>
<td>$R_{SS} [Ω]$ @ $V_{GS}=5.5, V_{DS}=0.05V$</td>
<td>47.92</td>
<td>32.03</td>
<td>20.45</td>
<td>31.88</td>
<td>36.79</td>
</tr>
<tr>
<td>$</td>
<td>\Delta R_{SS}</td>
<td>[Ω]$</td>
<td>13.66</td>
<td>6.62</td>
<td>0.64</td>
</tr>
<tr>
<td>$R_S [Ω]$</td>
<td>23.2</td>
<td>15.3</td>
<td>10.1</td>
<td>10.2</td>
<td>10.2</td>
</tr>
<tr>
<td>$</td>
<td>\Delta R_S</td>
<td>[Ω]$</td>
<td>23.1</td>
<td>15.4</td>
<td>10.0</td>
</tr>
<tr>
<td>$R_D [Ω]$</td>
<td>&lt;±1%</td>
<td>&lt;±1%</td>
<td>&lt;±1%</td>
<td>&lt;±1%</td>
<td>&lt;±1%</td>
</tr>
<tr>
<td>$</td>
<td>\Delta R_D</td>
<td>[Ω]$</td>
<td>&lt;±1%</td>
<td>&lt;±1%</td>
<td>&lt;±1%</td>
</tr>
<tr>
<td>$R_{TOT} [Ω]$</td>
<td>96.6%</td>
<td>95.8%</td>
<td>98.3%</td>
<td>63.0%</td>
<td>56.0%</td>
</tr>
<tr>
<td>$R \times W$ [MΩ cm]</td>
<td>9.3</td>
<td>12.3</td>
<td>12.1</td>
<td>12.1</td>
<td>12.4</td>
</tr>
</tbody>
</table>
characterization for each device and the result is summarized in Table I. Small changes in $V_T$ and $SSW$ are expected due to the hot carrier stress during the hot source characterization with the avalanche multiplication process for $V_{DS}>V_{DQ}$, but we observed no considerable drift in the parameters. This is because AHSM can be performed only once or twice in order to extract $RD$.

These results show that separated $R_S$ and $R_D$ are extracted consistently by the AHSM without causing any significant device performance degradation during characterization.

IV. CONCLUSIONS

We proposed a new technique for separated extraction of $R_S$ (source resistance) and $R_D$ (drain resistance) in MOSFETs considering possible asymmetries in layout, process variation and long term degradation of MOSFETs. It was named as “Avalanche Hot Source Method” because the high field region near the drain at a high drain voltage ($V_{DS}$) works as a new carrier source of excess EHP’s and the extra drain current $I_{D,hot}$ due to avalanche multiplication governing the current-voltage relation in MOSFETs with parasitic $R_S$ and $R_D$. Under avalanche multiplication, the drain current is limited by $R_D$ in MOSFETs and we obtained $R_D$ from the slope of $I_D$-$V_{DS}$ curves in the avalanche hot carrier-dominant operation region at a high $V_{DS}$. We applied the AHSM to n-channel MOSFETs with several $W/L$ combinations and verified its usefulness in the extraction of separated $R_S$ from $R_D$. We also confirmed that there was no considerable drift in $V_T$ and $SSW$ even after application of the method to MOSFETs under test with practical conditions.

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