A Range-Scaled 13b 100 MS/s 0.13 um CMOS SHA-Free ADC Based on a Single Reference

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Abstract—This work describes a 13b 100 MS/s 0.13 um CMOS four-stage pipeline ADC for 3G communication systems. The proposed SHA-free ADC employs a range-scaling technique based on switched-capacitor circuits to properly handle a wide input range of 2V_{P-P} using a single on-chip reference of 1V_{P-P}. The proposed range scaling makes the reference buffers keep a sufficient voltage headroom and doubles the offset tolerance of a latched comparator in the flash ADC1 with a doubled input range. A two-step reference selection technique in the back-end 5b flash ADC reduces both power dissipation and chip area by 50%. The prototype ADC in a 0.13 um CMOS demonstrates the measured differential and integral nonlinearities within 0.57 LSB and 0.99 LSB, respectively. The ADC shows a maximum signal-to-noise-and-distortion ratio of 64.6 dB and a maximum spurious-free dynamic range of 74.0 dB at 100 MS/s, respectively. The ADC with an active die area of 1.2 mm^2 consumes 145.6 mW including high-speed reference buffers and 91 mW excluding buffers at 100 MS/s and a 1.3 V supply voltage.

Index Terms—Analog-to-digital converter (ADC), pipeline, high resolution, SHA-free, range scaling, two-step reference selection

I. INTRODUCTION

Recently a variety of wireless communication systems, such as the 3G and 4G wide-band code division multiple access (W-CDMA), the wireless local area network (IEEE 802.11b), and the global system for mobile communication (GSM), have been developed corresponding to diverse user environments and needs. Along with the trend, high-performance analog-to-digital converters (ADCs) have been also highly demanded as an essential key building block in the system interface. Specifically, the ADCs for 3G communication system applications require at least 12b resolution and a conversion rate exceeding 65 MS/s with a small chip area and low power consumption.

Of various ADC architectures, the pipeline architecture has been commonly employed to meet the target specifications of 12b and 100 MS/s level [1-4]. Many inventive circuit techniques, such as the sample-and-hold amplifier (SHA)-free input network and signal range scaling, have been developed to obtain high signal-to-noise ratio (SNR) and low power dissipation of the pipeline ADCs operating at a low supply voltage [5-10]. On the other hand, with the state-of-the-art MOS processes still in progress, the decreased supply voltage tends to degrade the performance of analog circuits and particularly the available swing range of input and output signals of an operational amplifier (op-amp) is considerably limited. From a thermal-noise point of view, a reduced input full-scale range in half requires four times as large a sampling capacitance in the SHA for the same SNR performance, which increases the overall power consumption rapidly. Some range-scaling
techniques can remove the power-hungry input SHA while handling a wide signal swing range even at a low supply voltage [8-10]. A previously reported range scaling [8] needs dual reference voltages to process two different signal ranges of a large-swing off-chip input and a half-swing on-chip signal. As a result, somewhat complicated circuit schemes are accompanied to calibrate a mismatch between the two different reference voltages. The alternative range-scaling scheme [9] only employs a single reference voltage without extra calibration. However, since the input full-scale range is twice as large as the internally processed signal range, a single reference corresponding to the input full-scale range needs to be generated. This may limit the operating voltage headroom of the reference driver circuits at a low supply voltage.

This work proposes a 13b 100 MS/s SHA-free CMOS pipeline ADC based on a range-scaling scheme for a 2V_{P-P} input signal at a 1.3 V supply voltage. The proposed range-scaling scheme needs only a single reference voltage as large as the internally processed signal range, which corresponds to half of the full-scale input range. Thus, the buffers to drive the single reference voltage have sufficient dynamic voltage headroom even at a low supply voltage simultaneously with low power and a small chip area. Since the range scaling based on switched-capacitor circuits doubles the offset tolerance of a comparator in the first-stage flash ADC, it is possible to use a latched comparator without a pre-amp. As a result, extra timing circuits are not required for high input sampling accuracy as frequently observed in conventional SHA-free ADCs. In the back-end 5b flash ADC, the interpolation and two-step reference selection techniques reduce the required number of pre-amps and digital latches by about 50% with the corresponding chip area and power consumption.

The remainder of this paper is organized as follows. The range-scaling techniques for high-resolution pipeline ADCs are discussed in Section II. The proposed ADC architecture and detailed circuit implementation are described in Sections III and IV, respectively. The measured results of the prototype ADC are summarized in Section V and the conclusion is given in Section VI.

II. RANGE SCALING TECHNIQUES

Recently, decreasing supply voltages along with continuously developing fine-line CMOS technologies have limited the available signal operating range of op-amp-based circuits whereas the thermal and flicker (1/f) noise are not reduced as much. Considering the degraded dynamic range, a variety of range-scaling techniques without employing an input SHA have been invented for high-speed high-resolution low-power pipeline ADCs to handle a wide input range at a low supply voltage [8, 9]. A previously reported range scaling [8] adopts two pairs of reference voltages for two different signal swing ranges in a single ADC, as shown in Fig. 1(a). The higher reference voltages, V_{HREFT} and V_{HREFC}, are needed only in the first pipeline stage for a wide input signal swing, while the other reference voltages, V_{REFT} and V_{REFC}, are employed in the remaining pipeline stages for an attenuated signal swing. This scheme is essentially followed by an extra calibration technique to compensate for the mismatch between the two reference pairs, which degrades the overall ADC performance.

On the other hand, wide-band on-chip reference

![Fig. 1. Previous range-scaling techniques: based on (a) dual reference voltages [8] and (b) a single reference voltage [9].](image-url)
buffers are usually required to provide stable reference voltages to critical functional circuit blocks such as the multiplying digital-to-analog converters (MDACs) and flash ADCs operating at high speed and high resolution. These buffers should have a high enough voltage headroom between the reference and supply voltages for reliable operation. However, the buffers for the higher reference voltages, $V_{HREF_T}$ and $V_{HREF_C}$, have limited voltage headroom at a low supply voltage, as illustrated in Fig. 1(a). Furthermore, four power-hungry reference driving buffers increase the power consumption of the overall ADC considerably. The alternative range-scaling technique [9] is based on only two reference buffers without calibration and a single pair of reference voltages, $V_{REFT}$ and $V_{REFC}$, which are twice as wide as an internal signal swing. However, the voltage headroom of reference buffers at a low supply voltage is still limited, as shown in Fig. 1(b). Thus, the ADC employs external power supplies for the required reference voltages.

The proposed range-scaling technique, as illustrated in Fig. 2, properly processes input signals twice as wide as an internal signal range with only a pair of lower-level on-chip reference voltages, $V_{REFT}$ and $V_{REFC}$. The high-level reference voltages corresponding to the input signal range are needed only in the first pipeline stage and are generated from $V_{REFT}$ and $V_{REFC}$ by simple switched-capacitor circuits as discussed in Section IV. With this scheme, the required wide-band reference buffers have sufficient voltage headroom at a low supply voltage with reduced power dissipation and die area. There is also no need of additional reference calibration.

### III. PROPOSED ADC ARCHITECTURE

The proposed 13b four-step pipeline ADC is shown in Fig. 3. The first pipeline stage decides 3 bits while the second and third stages decide 4 bits, followed by the remaining 5 bits from the back-end flash ADC. The conventional input SHA is removed in this work while a range-scaling technique is employed in the first pipeline stage to handle a wide input range of $2V_{P-P}$ at a low supply voltage. The remaining pipeline stages are based on an attenuated signal swing of $1V_{P-P}$ for a stable operation with a high swing margin at a 1.3 V supply voltage. The ADC employs only a pair of on-chip reference voltages, $V_{REFT}$ and $V_{REFC}$, corresponding to $1V_{P-P}$. Switched-capacitor circuits double the reference levels for the $2V_{P-P}$ input in the first pipeline stage.

An input signal is directly sampled on the capacitors of the MDAC1 and flash ADC1 since there is no input SHA. A pre-amp is commonly employed in the flash ADCs to minimize the static and dynamic offsets of a latched comparator. However, the pre-amp in this SHA-free architecture may produce a sampling voltage mismatch between the MDAC1 and flash ADC1 due to the time delay for a pre-amp to amplify the difference between an input signal and a reference voltage. Although this problem can be solved with additional timing control circuits [6, 7], such a solution would increase the overall system complexity. Since the proposed range-scaling technique based on a single reference doubles the reference level in the first pipeline stage, the available input signal swing is also doubled. Thus, a simple latch-based comparator without a pre-amp properly resolves the 3b resolution in the flash ADC1 and the SHA-free input network does not suffer from the conventional sampling time mismatch. A gate-bootstrapping circuit for high linearity is also employed for sampling switches in both the MDAC1 and flash ADC1 [11]. The size ratio of the capacitors and switches in the input sampling
network is carefully designed to obtain the same RC time constant. In the back-end 5b flash ADC, two-step reference selection and interpolation schemes reduce both power and chip area further [12].

IV. CIRCUIT IMPLEMENTATION

1. MDAC1 for the Proposed Range-Scaling Technique

In conventional pipeline ADCs with the same signal range for input and reference voltages, for example, a 3b MDAC1 commonly amplifies a residue voltage by $2^2$ with four sampling capacitors and a feedback capacitor considering decision error correction from the flash ADC1. In contrast, the 3b MDAC1 for the proposed range scaling amplifies a residue voltage by 2 rather than $2^2$ with four sampling capacitors and a feedback capacitor, as shown in Fig. 4. During the sampling phase, an analog input is sampled on only two sampling capacitors, while the remaining two sampling capacitors and a feedback capacitor are reset to a common-mode voltage ($V_{\text{CM}}$), as shown in Fig. 4(a). During the next amplifying phase, reference voltages are connected to all the sampling capacitors corresponding to the digital code from the flash ADC1 while the feedback capacitor is connected to the amplifier output, as shown in Fig. 4(b). By sharing the sampled charge of four sampling capacitors, the signal gain of the MDAC1 is halved. At this point, the on-chip reference voltages, $V_{\text{REFT}}$ and $V_{\text{REFC}}$, are applied to the sampling capacitors to handle an input signal swing twice as wide as the internal reference range.

Since the proposed 3b MDAC1 amplifies a residue voltage by 2 rather than $2^2$, an input signal of $2V_{\text{p-p}}$ needs to be scaled down to $1V_{\text{p-p}}$ for the next pipeline stages. The remaining pipeline stages are implemented with the conventional topology. Each sampling capacitor is divided into two capacitor groups and each group consists of four smaller unit capacitors. Two groups of sampling capacitors for input and common-mode voltages are inter-digitated for layout to average out a mismatch error between the capacitors during the amplifying phase, as illustrated in the upper side of Fig. 4(a).

2. Flash ADC1 with Improved Offset Tolerance

The input switched-capacitor circuits for the flash ADC1 in the previous range-scaling scheme employ a single on-chip reference with an input range twice as wide as the reference [10], as illustrated in the single-ended version of Fig. 5(a). During the Q2 phase, a reference voltage is sampled in two separate sampling capacitors while the comparator input is reset to a signal common, $V_{\text{CM}}$. During the next Q1 phase, an input signal is applied to only one sampling capacitor while the other capacitor is connected to $V_{\text{CM}}$. Although the input range is twice as wide as the on-chip reference, at the comparator input, half of the input signal and the reference voltage are compared corresponding to the capacitor ratio as summarized in Fig. 5(b). As a result, the comparators in the flash ADC1 need a pre-amp with sufficient gain and bandwidth considering inherent latch offsets. The pre-amp itself may produce some undesirable sampling voltage mismatch between the
In contrast, the 3b flash ADC1 in this work doubles the required 8 reference levels to handle input signals twice as wide as the on-chip reference, as shown in Fig. 6. Thus, the comparators for the proposed range-scaling scheme have twice the offset tolerance compared with those for the conventional scheme while a simple latched comparator without a pre-amp can be employed.

The proposed 3b flash ADC1 consists of 16 synthesized reference generators, from X<0> to X<15>, and 8 latched comparators, from Y<0> to Y<7>, as shown in Fig. 7. Each reference generator produces an output signal, V<sub>OUTX</sub>, from two pairs of references and inputs. Two reference values are selected from V<sub>REFT</sub>, V<sub>REFC</sub>, and V<sub>CMLR</sub>, while two input values are selected from V<sub>INT</sub>, V<sub>INC</sub>, and V<sub>CM</sub>. The reference generator is actually implemented only with capacitors and MOS switches, as drawn in Fig. 8. The back-end latched comparators properly process an analog input of twice the on-chip reference range with 16 synthesized reference levels based on two pairs of input combinations.

During the Q2 clock of Fig. 8, two references of REF1 and REF2 are sampled in the sampling capacitors. During the next Q1, two inputs of IN1 and IN2 are connected to the same capacitors. Then, the output voltage, V<sub>OUTX</sub>, of the reference generator is derived as (1). In the case of X<0>, two reference inputs, REF1 and REF2, are connected to V<sub>CMLR</sub> while two signal inputs, IN1 and IN2, are connected to V<sub>INC</sub> and V<sub>CM</sub>, respectively. As a result, the output voltage, V<sub>OUTX</sub><~X<0~>, is calculated as (2). By repeating a similar process in the remaining reference generators with the appropriate reference and input pairs, all of the required 16 reference

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**Fig. 5.** Previous range-scaling scheme in the 3b flash ADC1 (a) circuits, (b) final reference levels.

**Fig. 6.** Reference levels of the 3b flash ADC1 for the proposed range scaling.

**Fig. 7.** Proposed 3b flash ADC1.

**Fig. 8.** Reference generator circuit.
levels are synthesized. The detailed input combinations for each reference generator are summarized in Table 1.

\[
V_{\text{OUT}} = \frac{IN1 + IN2}{2} - \frac{REF1 + REF2}{2} + V_{\text{CM}} \quad (1)
\]

\[
V_{\text{OUT}} < 0 > = \frac{1}{2} V_{\text{INC}} - V_{\text{CM}} + \frac{3}{2} V_{\text{CM}} \quad (2)
\]

Four outputs from the 16 synthesized reference output voltages in Fig. 7, \(V_{\text{OUT} < 0:15>}\), are properly applied to the 8 back-end latched comparators, as shown in Fig. 9. Then, the differential output of a comparator, \((LP-LN)\), is derived as (3) and an analog input is compared with 8 reference levels within \(\pm 2(V_{\text{REFL}} - V_{\text{REFC}})\) for a 3b resolution. The final complementary comparator outputs, \(T<0:7>\) and \(C<0:7>\), are transferred to the MDAC1 through digital output buffers. The detailed inputs and outputs of each latched comparator are summarized in Table 2.

\[
LP - LN = A0 \times \left(\left(LIN1 - LIN2\right) - \left(LIN3 - LIN4\right)\right)
\]

(\text{where, } A0 = \text{ comparator gain})

However, when a latch-based comparator without a pre-amp is employed in the pipeline ADCs, some amount of kick-back glitch noise can be generated in the output and referred to the input of the flash ADC due to a parasitic capacitance between the input and output nodes of the latch during the quantization process. The input-referred kick-back noise degrades the output signal settling time of the previous stage, disturbs the synthesized reference voltage levels, and ultimately affects the overall system accuracy. Two pull-down switches between the input differential pair and the regeneration nodes reduce the kick-back noise effect for improved comparison accuracy \([13]\).

3. Comparison of Various Range-Scaling Techniques

The proposed and some previously reported range-scaling techniques are compared in Table 3. A previous range-scaling scheme \([8]\) shows a design efficiency of an op-amp due to the doubled feedback factor and the reduced number of capacitors. However, extra reference buffers to drive two different pairs of reference voltages dissipate considerable power while some complicated calibration circuits, for matching two correlated reference pairs, are essential for high accuracy.

The alternative range-scaling scheme \([9]\) does not employ additional capacitors in the MDAC1 while the number of the MDAC capacitors in the remaining
pipeline stages needs to be doubled in order to scale down the reference voltage of the first stage MDAC by half. This technique needs a high dynamic range of reference voltage corresponding to the input, and actually employs the noisy power supply as a reference voltage due to limited voltage headroom of the reference driving buffers at a low supply voltage. The other range-scaling scheme based on a single reference [10] appropriately processes input signals twice as wide as the internal signal swing with a sufficient voltage headroom in the reference buffer circuits. However, the number of sampling capacitors required in the MDAC1 and flash ADC1 is doubled. Moreover, the comparator offset tolerance is reduced by half compared with other schemes since an input signal to the comparators in the flash ADC1 is reduced as much. Thus, the comparators in the flash ADC1 may need a pre-amp with a sufficient gain considering latch offsets, but the additional pre-amp itself can cause a sampling mismatch between the MDAC1 and flash ADC1 as observed in the conventional SHA-free range-scaled ADCs.

The proposed range-scaling technique doubles the number of capacitors in the flash ADC1 while a resistor string consuming a DC current in the flash ADC1 is not needed. The reference buffers have sufficient voltage headroom since the proposed scheme employs only a single on-chip reference voltage corresponding to half of the input signal range. The comparators of the flash ADC1 in the first pipeline stage compare an input signal with the reference levels increased by twice based on the switched-capacitor circuits. Due to the doubled offset tolerance in the comparator, a latched comparator without a pre-amp can be used in the flash ADC1 without additional timing circuits for high input sampling accuracy.

V. ADC IMPLEMENTATION AND MEASUREMENTS

The prototype 13b 100 MS/s ADC is implemented in a 0.13 um CMOS technology, as shown in Fig. 10. The ADC occupies an active die area of 1.2 mm² including on-chip MOS decoupling capacitances of about 250 pF. The ADC dissipates 145.6 mW including on-chip reference buffers and 91 mW excluding buffers at 100 MS/s and a 1.3V supply voltage.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are within ±0.57LSB and ±0.99LSB, respectively, as shown in Fig. 11. A typical signal spectrum at 100 MS/s with a 4 MHz input sine wave is plotted in Fig. 12. Digital output data are captured at a quarter rate of the full conversion speed of 100 MS/s with the on-chip decimator.

The signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) in Fig. 13(a) are measured with sampling frequencies from 10 MHz to...
While a sampling frequency increases to 100 MHz, the SNDR and SFDR are maintained above 64.6 dB and 74.0 dB, respectively. The SNDR and SFDR variations with increasing input frequencies at a maximum sampling rate of 100 MS/s are illustrated in Fig. 13(b). The SNDR and SFDR are maintained over 50.4 dB and 64.0 dB, respectively, at the Nyquist input frequency. The dynamic performance of the ADC is rapidly degraded with increasing input frequencies due to a sampling time mismatch between the MDAC1 and flash ADC1 as commonly observed in the conventional SHA-free topology. The prototype ADC under revision is expected to show much improved dynamic performance at high input frequencies by integrating digitally controllable sampling time-delay circuits at the input stage.

The figure of merits (FoM), defined as (3), of the prototype ADC is 0.66 pJ/conversion-step excluding on-chip reference buffers. The recently reported CMOS ADCs with a resolution above 12 b and a sampling clock rate exceeding 70 MS/s are compared with the proposed ADC in Fig. 14 and the overall ADC performance is summarized in Table 4.

\[
FoM = \frac{\text{Power}}{2^{\text{ENOB}} \times f_s}
\]  

VI. CONCLUSIONS

This work proposes a 13b 100 MS/s 0.13 um CMOS ADC for 3G W-CDMA applications. The ADC employs an input SHA-free four-step pipeline architecture to achieve high-resolution, low power, and small die area at
a sampling rate of 100 MS/s. The proposed range-scaling scheme, using switched-capacitor circuits, properly handles an input signal range twice as wide as an on-chip signal swing based on a single reference voltage. The reference buffers have sufficient dynamic voltage headroom at a low supply voltage. Since the proposed technique doubles the offset tolerance of latched comparators, the flash ADC without a pre-amp decides 3b resolution. The prototype ADC shows a maximum DNL and INL within 0.57LSB and 0.99LSB, respectively. The ADC shows a maximum SNDR of 64.6 dB and a maximum SFDR of 74.0 dB at 100 MS/s, respectively. The ADC with an active die area of 1.2 mm\(^2\) consumes 145.6 mW including on-chip reference buffers and 91 mW excluding reference buffers at 100 MS/s and a 1.3 V supply voltage.

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