Device and Circuit Level Performance Comparison of Tunnel FET Architectures and Impact of Heterogeneous Gate Dielectric

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Abstract—This work presents a comparative study of four Double Gate tunnel FET (DG-TFET) architectures: conventional p-i-n DG-TFET, p-n-p-n DG-TFET, a gate dielectric engineered Heterogate (HG) p-i-n DG-TFET and a new device architecture with the merits of both Hetero Gate and p-n-p-n, i.e. HG p-n-p-n DG-TFET. It has been shown that, the problem of high gate capacitance along with low ON current for a p-i-n TFET, which severely hampers the circuit performance of TFET can be overcome by using a p-n-p-n TFET with a dielectric engineered Hetero-gate architecture (i.e. HG p-n-p-n). P-n-p-n architecture improves the ON current and the heterogeneous dielectric helps in reducing the gate capacitance and suppressing the ambipolar behavior. Moreover, the HG architecture does not degrade the output characteristics, unlike the gate drain underlap architecture, and effectively reduces the gate capacitance.

Index Terms—Ambipolar, hetero gate (HG), p-i-n, p-n-p-n, propagation delay, tunneling field-effect transistor (TFET)

I. INTRODUCTION

With the CMOS technology facing incessant challenges in the sub 100 nm regime, the research focus has been shifted to the investigation of novel device architectures that can overcome the limitations of power supply scaling with device dimensions and works on current conduction mechanisms other than thermionic emission by potential barrier lowering. The tunnel FET has been given much attention in this regard as an alternative device architecture exhibiting a subthreshold swing (SS) below the conventional limits of MOSFET i.e. 60mV/dec, a low leakage current, suppressed Short Channel Effects (SCE) [1, 2] and CMOS compatible process flow [3]. Numerous device designs and optimization techniques (both experimental and simulation based) such as strain engineering, hetero-junction architectures, usage of low bandgap materials, tunnel source MOSFET [4-9], have been proposed in recent years in order to improve upon the shortcomings of TFET (a low ON current being the major bottleneck). With recent work reported on the enhanced ON current, TFET has emerged out as an attractive contender for future low power supply technology nodes. The basic structure for a TFET is gated p-i-n diode configuration working in reverse bias. In order to overcome low ON current problem and have effective gate modulation to improve tunneling probability, a modified architecture i.e. p-n-p-n (also known as tunnel source MOSFET) was proposed [9], with a heavily doped n-type layer between the source and channel forming an abrupt and heavily doped tunnel junction. Another problem prevalent in

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Fig. 1. Schematic of simulated device architectures (a) p-i-n, (b) Hetero Gate p-i-n (HG p-i-n), (c) p-n-p-n, (d) Hetero Gate p-n-p-n (HG p-n-p-n). All the architectures are shown to be working in n-type operation. For p-type operation the source doping is n type (n+) and drain doping is p type (p+). Parameters: Source doping $N_A=10^{20} \text{ cm}^{-3}$, drain doping $N_D=10^{20} \text{ cm}^{-3}$, $N_{ch} (p)=10^{15} \text{ cm}^{-3}$, pocket doping (N_p)= $5 \times 10^{19} \text{ cm}^{-3}$, channel length $L_{ch}=45 \text{ nm}$, pocket width $L_p=3 \text{ nm}$, oxide thickness (t_{ox})= 3 nm , $t_{si}=10 \text{ nm}$.

TFETs is ambipolar conduction [10]. In order to overcome this impediment, the Hetero Gate (HG) dielectric TFET was proposed by Choi *et. al* [11], which is capable of suppressing the ambipolar device characteristics due to the presence of a low-k gate dielectric material at the drain end. There are several other methods reported to suppress this ambipolar behavior such as: asymmetric source/drain doping [12], gate drain underlap or short gate TFET [13, 14] and hetero-junction TFET [15] being the most extensively studied. The later scheme i.e. short gate/gate drain underlap is also effective in reducing the gate-drain capacitance, which is very high in case of TFETs and leads to inferior circuit performance [16], but it has its implications on increasing channel resistance [13] and degrading the output characteristics [17]. Thus, in this work, a gate dielectric engineered Hetero gate (HG) p-i-n and p-n-p-n architecture are taken into consideration, in order to study the impact of gate dielectric modulation on ambipolar behavior and more importantly on the device capacitance characteristics and circuit performance. As far as the experimental realization of the p-i-n, p-n-p-n and HG TFET architectures are concerned, a Double Gate architecture has already been demonstrated experimentally [7] for a conventional p-i-n TFET structure. The fabrication process steps for a p-n-p-n

architecture are reported in literature, wherein a tilt angled implant is used to form heavily doped pocket after gate definition [9]. The Hetero-gate TFET can be achieved by isotropic etching of low-k material and then deposition of high-k gate oxide as reported in [11]. In view of the various fabrication methods, reported for p-n-p-n and Hetero gate dielectric TFET structures, it seems feasible to realize the proposed Hetero-Gate (HG) p-n-p-n TFET with the fabrication techniques discussed above. In the present work, a comparative study of four different TFET architectures viz. p-i-n, HG p-i-n, p-n-p-n and HG p-n-p-n in terms of their static, dynamic and circuit level performance is carried out through exhaustive device and circuit simulation.

II. SIMULATION AND CALIBRATION

1. Device Architecture and Parameters

Device structures considered in this study are conventional p-i-n TFET, Hetero Gate dielectric p-i-n TFET, p-n-p-n TFET and a new architecture amalgamating the benefits of Hetero Gate and p-n-p-n both i.e. Hetero Gate (HG) p-n-p-n DGTFET (Fig. 1). A Double Gate geometry is considered with channel length of 45 nm, silicon film thickness $t_{si}=10 \text{ nm}$, high-k gate

oxide thickness t_{ox} of 3 nm ($\epsilon_{ox}=21$) for all the device architectures. The source and drain doping are assumed to be symmetric (10^{20}cm^{-3}) to highlight the impact of a HG structure on ambipolar conduction. The length of high-k ($\epsilon_{ox1}=21$) material is 25 nm and that of low-k material ($\epsilon_{ox2}=3.9$ SiO_2) is 20 nm for a Hetero-Gate structure. For p-n-p-n and HG-p-n-p-n structure, an n+ heavily doped pocket of width 3 nm located at the source/channel junction is used, thus making the total gate length to be 48 nm, and hence keeping the channel length ($L_{ch}=45$ nm) to be identical in all four cases. The pocket doping is taken as $5 \times 10^{19} \text{ cm}^{-3}$ such that the 3 nm of pocket width always remains fully depleted in order for p-n-p-n TFET to work properly [9]. The source and drain junctions are assumed to be abrupt, as with some of the recently reported techniques such as Plasma doping (PLAD) and Excimer Laser Annealing (ELA), it is possible to obtain abrupt junctions [18, 19]. With a recently proposed technique (dopant profile-steepening implant (DPSI)) [20] it is possible to achieve a doping gradient as steep as 1 nm/dec, resulting in almost abrupt tunneling junction and alleviating the problem of doping smear out at the tunneling junction. For a p-n-p-n architecture, it is assumed that, with a local doping gradient as steep as 1 nm the junction formed between p+ source and n type heavily doped pocket can be assumed abrupt. In order to make a performance comparison between different architectures all four devices are optimized to have similar off current (I_{off}) of 0.1 pA/ μm (below the ITRS limit). In order to do so, the gate metal work function is varied. The drain supply voltage V_{DD} is considered to be 1 V for the 45 nm node.

2. Calibration of TFET model

The non local Band-to-Band Tunneling (BTBT) Model available in Silvaco ATLAS [21] is calibrated [22] with the experimental data available for Si NW TFET [23]. The tunneling masses are adjusted from their default value (i.e. $m_e=0.322$, $m_h=0.549$ in ATLAS) to attain the best fit with the experimental results. The best fit is obtained for the combination $m_e=0.4$ and $m_h=0.52$. Along with non-local BTBT model, the physical models activated during device simulations are: Schokley Read Hall (SRH) recombination model, concentration and field dependent mobility models, Hurkx recombination model

and band gap narrowing (BGN). To take into consideration the non-stationary transport effects that become inevitable in sub-100 nm region, energy balance transport (EBT) model is activated.

As will be discussed in Section III, that the activation of EBT model does not bring a significant change in the I_{ds} - V_{gs} characteristics, thus obscuring its inclusion. Moreover, the agreement between the characteristics obtained through Drift Diffusion model (with ATLAS default parameters) and the Monte Carlo (MC) results [24] are quite good for transistors down to 40 nm gate lengths. Thus, the conventional drift diffusion (DD) model is used, which happens to be less time consuming as well.

III. DC PERFORMANCE COMPARISON

1. Energy Band Diagram

The impact of different architectures on the energy band diagram (in OFF state) is depicted in Fig. 2(a). Due to the presence of a low-k gate oxide near the drain end of TFET, the barrier width at the drain end further increases which helps in reducing the ambipolar behavior which has its implication in forming a complementary TFET (p-TFET) and also on the circuit performance. The ambipolar conduction becomes an issue of major concern for TFETs, when it is configured in circuit topology. For a Hetero Gate (HG) p-n-p-n structure the ambipolar behavior reduces as compared to a p-n-p-n structure as shown in Fig. 3(a).

The barrier width formed at the source-channel junction is reduced for a p-n-p-n and HG p-n-p-n TFETs while the drain end of HG p-n-p-n has much wider barrier owing to heterogeneous gate dielectric. This improvement in ambipolar conduction suppression can also be observed by the amount of reduction in electric field at the drain end, due to the presence of a low-k dielectric as shown in Fig. 2(b). Thus, when the device is in OFF state, the band-to-band tunneling (BTBT) at the drain end which leads to ambipolar current can be effectively suppressed with a heterogeneous dielectric configuration.

2. I_{ds} - V_{gs} and I_{ds} - V_{ds} Characteristics

As already mentioned in the model calibration part,

Fig. 2. (a) Energy Band diagram along the channel in the off state. Band bending at source side is more for a p-n-p-n architecture and barrier width at drain end increases due to HG structure. Straight line indicates start and end of channel region for p-i-n and p-n-p-n structure, (b) Electric field plotted across the channel length for all the architectures showing the impact of HG in reducing the field at the drain end.

that using Energy Balance Transport for simulations does not bring a significant change in the device characteristics. In this context, Fig. 3(a) (inset) compares the current voltage characteristics obtained from DD and EBT model and they are found to be similar and in close proximity to each other and thus validates the choice of Drift Diffusion model. Fig. 3(a) compares the TFET architectures for their I_{ds} - V_{gs} characteristics. The On

Fig. 3. (a) I_{ds} - V_{gs} characteristics for different TFET architectures depicting the ambipolar characteristics. (Inset) Comparison of Current Voltage Characteristics obtained through Drift Diffusion (DD) and Energy Balance Transport (EBT) model for a p-i-n TFET, (b) I_{ds} - V_{ds} characteristics for all TFET architectures at V_{gs} (=0.6V) and V_{gs} (=1V). At lower gate overdrive, the drain saturation voltage is small.

current (I_{ON}) for a p-n-p-n architecture is enhanced in comparison to p-i-n due to a heavily doped n+ pocket region present at the source channel junction, which helps in improving the lateral electric field appearing at the tunneling junction and hence the drive current.

It has been observed that the p-i-n and HG p-i-n structure and similarly p-n-p-n and HG p-n-p-n structure have identical I_{ds} - V_{gs} and I_{ds} - V_{ds} characteristics (Fig. 3(a),

(b)), for positive gate bias values ($V_{gs} > 0$, for n type TFET configuration). But, the difference in their behavior lies in negative gate bias region ($V_{gs} < 0$) while studying the ambipolar conduction, which shows the advantage of using a hetero gate structure. Due to the presence of a low- k dielectric at the drain end, the ambipolar current has reduced (Fig. 3(a)) by about 4 orders. The I_{ds} - V_{ds} characteristics are shown in Fig. 3(b). As expected the p-n-p-n architecture offers high drain current. Fig. 3(b) shows that TFET exhibits delayed saturation effect i.e. the drain current saturates at high V_{ds} (V_{dsat} is high) for higher gate bias. This is because at high V_{gs} when the channel is in inversion condition, a large part of V_{ds} drops at the tunnel junction and the tunnel barrier width keeps on changing for large range of V_{ds} values till it gets saturated. Once the barrier width reduction saturates the channel starts pinching-off at the source side and drain current starts to saturate leading to a high drain saturation voltage (V_{dsat}). Thus, the saturation point keeps on shifting to higher V_{ds} values for high V_{gs} and as the gate overdrive is reduced the drain saturation voltage also decreases (Fig. 3(b) (inset)).

As reported by Verhulst *et al.* [13], that gate drain underlap (GDU) structure results in a higher channel resistance under the non-gated region. This high series resistance does not affect the dc performance at low gate bias values where the dominating mechanism is the reduction of tunnel barrier width. The role of channel resistance comes into play at high V_{gs} values for drain current saturation. Mallik *et al.* reported drain voltage influence on TFET characteristics [17] predicting an inferior drain-current (saturation) characteristics of gate drain underlap (GDU) structure in comparison to a TFET with full gate (aligned with both source and drain junction). However, when a Hetero gate structure is used for both p-i-n and p-n-p-n, the output characteristics does not change (Fig. 3(b)). Hence, HG architecture does not result in the variation of electrical parameters (ON current, subthreshold slope and even the threshold voltage) exhibited by the basic p-i-n and p-n-p-n structure, and shows its merit in ambipolar conduction suppression and also in the dynamic performance as will be discussed later in section V. It also overcomes the problems associated with GDU such as (a) degradation of drain current saturation characteristics, (b) a high resistance channel region due to non gated region. Thus,

it can be concluded that, in order to improve the performance of TFET, HG architecture can be considered as a better alternative as compared to GDU, since it provides all the advantages exhibited by GDU, with several other benefits as discussed above.

IV. DYNAMIC PERFORMANCE COMPARISON

1. Capacitance Voltage Characteristics

The degradation of device performance is mainly attributed to the presence of bias dependent parasitic components of capacitances C_{gs} and C_{gd} . Gate to drain capacitance (C_{gd}) is the most important among the gate capacitances because its effect is multiplied by the voltage gain between the drain and gate nodes due to Miller effect. The dynamic behavior of a device is the result of device capacitive effects caused by the charges stored in the device. The capacitive effects is the sum of intrinsic (channel) and extrinsic (source and drain junctions) capacitances [25]. As reported by Yang *et al.* [26] and Mookerjee *et al.* [16], the distribution of capacitance between source and drain in p-i-n TFETs is quite different in comparison to a MOSFET. In TFETs, at low V_{ds} values or even at high V_{ds} values, C_{gd} comprises the major part of the gate capacitance (C_{gg}) unlike MOSFETs. Thus, C_{gd} is the dominant component of gate capacitance, and this high value of C_{gd} (further enhanced due to Miller effect), poses a limitation on switching speed and power dissipation [27] of TFET based circuits. The limiting factor for attaining high cut-off frequency is the low value of trans-conductance and a high gate-to-drain capacitance (C_{gd}). In the present work, the comparison of C-V characteristics and the distribution of various capacitive components for all the architectures under consideration is analyzed (Fig. 4) and is correlated with the dynamic performance and the transient response of different device architectures.

The techniques already reported in order to reduce the Miller capacitance component C_{gd} are (a) use of an abrupt drain junction, (b) gradual drain junction with offset [26], (c) use of a gate drain underlap or short gate TFET [14], (d) use of a low bandgap material [16] etc.

The drain offset or the short gate structure results in a higher channel resistance near the drain region. For a Heterogeneous dielectric i.e. Hetero Gate p-i-n TFET the

Fig. 4. Capacitance component variation with gate voltage (V_{gs}) at two V_{ds} values (0, 1V) for (a) p-i-n, (b) Hetero Gate p-i-n (HG p-i-n), (c) p-n-p-n, (d) Hetero Gate p-n-p-n (HG p-n-p-n) extracted at $f=1$ MHz. Inset shows the contribution of C_{gs} and C_{gd} towards gate capacitance C_{gg} of all the architectures.

charge induced in the channel region near the drain is lower as compared to a p-i-n TFET with a single high-k gate dielectric. This is due to the presence of low-k dielectric and hence lower effective gate bias near the drain end. So, the gate capacitance and the gate drain capacitance component both are reduced significantly for HG p-i-n structure as shown in Fig. 4(a) and (b). Thus, Hetero gate architecture can effectively suppress both ambipolar behavior as well as the miller capacitance C_{gd} quite similar to the effect of short gate or gate drain underlap but without increasing the channel resistance. Further, it is interesting to notice that the gate source capacitance (C_{gs}) component is not negligibly small in comparison to gate drain capacitance (C_{gd}) in case of a p-n-p-n architecture and the overall gate capacitance (C_{gg}) is also lower than p-i-n for the same channel length. With the introduction of a hetero dielectric, the total gate capacitance C_{gg} is divided almost equally into C_{gs} and C_{gd} even in the saturation region in contrast to a MOSFET where C_{gs} and C_{gd} contributions are equal in the linear region and C_{gd} becomes negligible in the saturation region. Thus, we can see that there is a tremendous rise in the C_{gs} contribution as we move from a p-i-n

architecture to a p-n-p-n and the additional advantage provided through a hetero dielectric in further reducing the C_{gd} component.

In order to explain the difference in the distribution of capacitance components for different TFET architectures, electron concentration profile along the channel length is obtained (Fig. 5(a)). It has been observed that for p-n-p-n and HG p-n-p-n structures, the electron concentration profile is similar near the source-channel junction but the magnitude is higher than p-i-n and HG-p-i-n architecture due to the higher gate overdrive voltage (@ $V_{gs}=1V$) in case of p-n-p-n and HG p-n-p-n because of their lower threshold voltage. This results in enhanced C_{gs} component for p-n-p-n TFET. Similarly, the electron concentration profile is same for p-i-n and HG p-i-n at the source channel junction. However, the changes in the electron concentration profile occurring at the drain junction which leads to difference in the C_{gd} component is mainly because of the HG structure due to which the charge induced at the drain junction is minimum for a HG p-n-p-n structure and hence it has got the minimum gate capacitance and gate drain capacitance component. The percentage reduction in C_{gd} with respect to p-i-n

Fig. 5. (a) Electron concentration distribution in the channel region in saturation regime ($V_{gs}=V_{ds}=1$ V), (b) Cut off frequency (f_T) variation with gate-source voltage (V_{gs}) for the four TFET architectures and MOSFET (inset) under study.

architecture is 43%, 55% and 71% for HG p-i-n, p-n-p-n and HG p-n-p-n architecture respectively. The percentage increase in the C_{gs} component with respect to p-i-n is only 7.7% for HG p-i-n. Meanwhile, for p-n-p-n architecture the C_{gs} component increased by almost two times with respect to p-i-n and similarly three times for HG p-n-p-n architecture.

Thus, due to minimum gate capacitance in case of HG p-n-p-n structure, it exhibits higher cut-off frequency (f_T) (as shown in Fig. 5(b)). The maximum cut-off frequency

obtained are 36.7GHz, 52 GHz, 226 GHz and 273 GHz for p-i-n, HG p-i-n, p-n-p-n, and HG p-n-p-n TFET respectively. The advantage of HG architecture in enhancing the cut-off frequency [28] is attributed to the reduction in gate drain capacitance. Due to this reduction in C_{gd} , the denominator term in the expression used for

$$\text{cut-off frequency calculation } \left(f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \right)$$

decreases and hence results in higher value of f_T . The cut-off frequency obtained for a p-n-p-n TFET is even higher in comparison to recently reported values for a GAA p-i-n TFET [29], because of the enhancement in the transconductance (g_m) and reduction in C_{gd} for a p-n-p-n architecture in comparison to p-i-n. The cut-off frequency (f_T) shows a decreasing trend for $V_{gs} > 0.8$ V, although in case of TFET, the transconductance g_m does not saturate. This behavior is due to the increase in $(C_{gs} + C_{gd})$ factor with gate voltage which is much higher in comparison to increase of g_m . Thus the denominator increases by a higher factor as compared to numerator in the expression of f_T which results in the decreasing trend of cut-off frequency after $V_{gs} = 0.8$ V. Further, a HG p-n-p-n structure is expected to possess a minimum intrinsic delay and voltage overshoot as will be discussed in the next section on transient analysis.

Having compared the device level performance in terms of capacitive components, it is imperative to evaluate the circuit level performance as well for all the architectures. The next section deals with the circuit level performance comparison for an n-TFET resistive load inverter as shown in Fig. 6(a), and assessing the impact of different architectures through the transient response.

2. Transient Analysis

The voltage overshoot in the transient response of inverter circuit (Fig. 6(a)) is mainly attributed to the gate-drain capacitance (C_{gd}) of the inverter transistors, which directly couples the steep voltage step at the input node to the output even before the response of transistor. Since in case of TFET, the gate drain capacitance (C_{gd}) is large, so the voltage overshoot is very high for a p-i-n TFET (Fig. 6(c)). But, as already mentioned above that a Hetero gate structure effectively reduces C_{gd} , the reduction in the voltage overshoot is also observed (Fig.

Fig. 6. (a) n-TFET/n-MOS inverter with resistive load ($R=100$ Mohm) and (color online), (b) transient response for n-MOS inverter. (c), (d), (e), & (f) Transient response of n-TFET Inverter circuit with resistive load for load capacitance variation and the amount of fall propagation delay (t_{PHL}) and peak overshoot voltage (V_p) for all four TFET architectures.

6(c), (f)), which is more pronounced for a circuit with finite load capacitance value.

For a loaded circuit ($C_L=1, 10$ fF) the overshoot becomes negligibly small, but the disadvantage is the increase in the delay time. This problem can be addressed by the Hetero gate p-n-p-n architecture for which the peak overshoot voltage is minimum and also the introduction of a load capacitance does not increase the delay time drastically as is the case with p-i-n architecture.

The peak overshoot voltage and fall propagation delay

(t_{PHL}) corresponding to different architectures at different load capacitance (C_L) values are summarized in Fig. 6(b)-(f). The fall propagation delay (t_{PHL}) for an inverter is calculated as the delay time between the 50% input point to the 50% output point [30]. As mentioned earlier that a heterogeneous dielectric structure is effective in reducing the gate capacitance, and hence can be effective in reducing the delay time. It is quite apparent from Fig. 6 that incorporating a HG structure reduces the delay time for a p-i-n structure and as already mentioned above that a p-n-p-n structure has even a lower gate capacitance as compared to p-i-n, so a HG dielectric architecture on p-n-p-n reduces it further by around 4 times in comparison to p-i-n architecture.

V. CIRCUIT LEVEL PERFORMANCE COMPARISON

In order to assess the effect of different architectures on circuit level performance, circuit simulations are carried out for an inverter circuit, benchmark circuits such as five stage ring oscillator and chain of logic gate (i.e. 10 stage NAND gate) using table look up based model employing PETE (Purdue Exploratory Technology Evaluator) deployed on Nanohub [31, 32]. This tool is helpful in estimating the circuit performance of non-classical novel device architectures such as a TFET. A table look up model approach is used for TFET circuit simulation due to the unavailability of physics based compact analytical model for TFET. The circuit simulations on commercial device simulators does not work properly for TFET based complementary circuits [33], and an equivalent circuit [34] or a table look up model based approach is required to perform logic circuit analysis. This tool has already been used to study the device and circuit performance of carbon nanotube p-i-n TFET [35]. The input for the table look up based model are the I-V and C-V device characteristics obtained by 2D device simulations with very fine voltage steps of 0.02V and 0.1V for V_{gs} and V_{ds} respectively. The capacitance components are extracted at 1MHz frequency. Both p-type and n-type TFET [36] and MOSFET are optimized for similar off current (I_{off}) level by adjusting the gate metal work function. The work function for n-type devices are in the range of 4.1eV to 4.25 eV and those of p-type in 5.25 eV to 5.33 eV. To ascertain the

Fig. 7. (a) Schematic of Complementary TFET and MOSFET (C-TFET and CMOS) inverter circuit, (b) Comparison of Voltage Transfer characteristic (VTC) curve for CMOS inverter obtained through ATLAS device simulation and table look model from PETE [31].

accuracy of table look up based model in comparison to Physics based circuit simulation obtained through a commercial numerical simulator, characteristics of a CMOS inverter based on DG- MOSFET structure is studied (both dc and transient). The geometrical parameters are kept similar to that of TFET architecture used in this study and optimized for off current levels as mentioned above. The Voltage Transfer characteristics (VTC) curve for a CMOS inverter (Fig. 7(a)) obtained through PETE and ATLAS are shown in Fig. 7(b), and the characteristics matches well and the static noise margin (SNM) is similar from both the approaches (i.e 0.485V). Fig. 8 compares the VTC characteristics of four architectures obtained through complementary TFET (C-TFET) inverter simulation on Nanohub. As discussed

earlier in Section III, the inclusion of HG architecture for a p-i-n TFET does not result in the shift of the electrical characteristics and hence the dc characteristics of C-TFET inverter circuit are similar for p-i-n and HG p-i-n and for p-n-p-n and HG p-n-p-n. The static noise margin (SNM) of the TFET is lower in comparison to MOSFET, because of a high drain saturation voltage of TFETs as discussed in Section III.

The devices are being compared on the basis of propagation delay, switching energy, static and dynamic power dissipation for benchmark circuits such as combinational logic circuit i.e. 10 stage NAND and NOR chain, and 5 stage ring oscillator.

1. Delay

Delay time depends directly on the intrinsic capacitance and inversely to current. So as shown in Fig 9(a), the delay time for MOSFET is minimum since the current level is highest and the intrinsic capacitance component is also minimum for MOSFET. For an inverter circuit, HG p-n-p-n shows reduction in delay time from 72 ps (for p-i-n) to 12.7 ps (HG p-n-p-n) which is nearly 5.6 times due to its high current levels and low gate capacitance. Similarly for 10 stage NAND gate, NOR gates and 5 stage ring oscillator circuit, HG p-n-p-n exhibits lowest delay out of all TFET devices under consideration.

2. Static/Leakage Power

The amount of power dissipated due to leakage current is termed as static power dissipation. Since the off

Fig. 8. Voltage Transfer Characteristics (VTC) depicting the Static noise margin (NM_H and NM_L) for (a) p-i-n, (b) Hetero Gate p-i-n (HG p-i-n), (c) p-n-p-n, (d) Hetero Gate p-n-p-n (HG p-n-p-n).

Fig. 9. (a) Delay, (b) Dynamic power dissipation, (c) Static power dissipation for 10 stage NAND gate, NOR gate and 5 stage Ring oscillator for TFETs and MOSFET.

current for all the devices are optimized for similar levels ($0.1 \text{ pA}/\mu\text{m}$), so the static power dissipation is almost similar for all device architectures (Fig. 9(c)). However, if TFET architectures and MOSFET were not optimized to have similar off current levels, then for a particular gate work function value, TFETs would have outshined MOSFET in terms of static power dissipation due to the very low leakage current for TFET.

3. Dynamic Power Dissipation

Dynamic power dissipation is contributed by switching /charging, discharging of capacitances. Since the current level for MOSFET is highest, so its dynamic power dissipation is also high. Similarly, the ON current is higher for p-n-p-n and HG p-n-p-n in comparison to p-i-n and HG p-i-n structure, thus both the p-n-p-n and HG p-n-p-n architecture have higher power dissipation. It is important to note that, due to increase in ON current level and decrease in gate capacitance for p-n-p-n (Fig. 4) in comparison to p-i-n, the delay has reduced, but the dynamic power dissipation is still higher because the

enhancement in ON current dominates the reduction in gate capacitance. While for HG p-n-p-n, the current is similar to that of p-n-p-n, but due to reduction in gate capacitance (because of hetero gate dielectric) the delay reduces further without increasing the dynamic power dissipation. In fact, the dynamic power dissipation in HG p-n-p-n is slightly lower than the p-n-p-n architecture. Similar is the case with p-i-n and HG p-i-n, the delay reduces due to the effect of heterogeneous dielectric at almost similar power dissipation. Thus, a hetero gate structure is beneficial in improving the propagation delay without increasing the power dissipation with ambipolar conduction suppression. Another important aspect of HG architecture is that, if a complementary circuit is designed (having electrical parameters such as I_{ON} , I_{OFF} and V_{th}), the replacement of a p-i-n device with HG p-i-n, and similarly p-n-p-n with HG p-n-p-n is possible without any mismatch as the operating conditions will not change due to the usage of Heterogate dielectric. Infact, the circuit performance would improve as the capacitive load and the ambipolar conduction reduces, and the architectural advantage can be utilized optimally.

VI. CONCLUSIONS

An extensive investigation of four different TFET architectures for their static, dynamic and circuit level performance has been carried out. A new device architecture with gate dielectric engineered, i.e. combining the benefits of p-n-p-n and Hetero gate architecture termed as HG p-n-p-n is studied. It has been shown, that HG architecture is useful in suppressing the ambipolar conduction effectively, and most importantly lowers the gate capacitance and miller capacitance leading to reduced loading effect and hence lower power dissipation. Further, with the advantage of high I_{ON} for a p-n-p-n architecture in comparison to p-i-n, the propagation delay reduces and the high miller capacitance problem can be alleviated by heterogeneous gate dielectric.

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