A 12 mW ADPLL Based G/FSK Transmitter for Smart Utility Network in 0.18 µm CMOS

Hyung-Gu Park, Hongjin Kim, Dong-Soo Lee, Chang-Zhi Yu, Hyunchul Ku, and Kang-Yoon Lee

Abstract—This paper presents low power frequency shift keying (FSK) transmitter using all digital PLL (ADPLL) for smart utility network (SUN). In order to operate at low-power and to integrate a small die area, the ADPLL is adopted in transmitter. The phase noise of the ADPLL is improved by using a fine resolution time to digital converter (TDC) and digitally controlled oscillator (DCO). The FSK transmitter is implemented in 0.18 µm 1-poly 6-metal CMOS technology. The die area of the transmitter including ADPLL is 3.5 mm². The power consumption of the ADPLL is 12.43 mW. And, the power consumptions of the transmitter are 35.36 mW and 65.57 mW when the output power levels are -1.6 dBm and +12 dBm, respectively. Both of them are supplied by 1.8 V voltage source. The frequency resolution of the TDC is 2.7 ps. The effective DCO frequency resolution with the differential MOS varactor and sigma-delta modulator is 2.5 Hz. The phase noise of the ADPLL output at 1.8 GHz is -121.17 dBC/Hz with a 1 MHz offset.

Index Terms—FSK, transmitter, all-digital phase-locked loop (ADPLL), time-to-digital converter (TDC), digitally controlled oscillator (DCO), two-step TDC, phase-interpolator, time amplifier

I. INTRODUCTION

IEEE 802.15.4g is a recent standard for SUN (smart utility network) which is considered to be one of the most important applications of low-power radio systems [1].

In the SUN system, low power consumption and die area are becoming more and more important to increase battery life and reduce system cost. Supply voltage is lowered as the minimum feature size of the process is scaled. Thus, the concept of a digital circuit can be adopted when a conventional analog circuit currently faces difficulty nowadays. Digital circuits have several advantages over conventional analog circuits in terms of scalability with the supply voltage, immunity to noise, and wide operating range.

All-digital phase-locked loop (ADPLL) architectures for digital RF transceivers are becoming attractive in submicron technology. An ADPLL uses a TDC instead of a charge-pump. The use of the TDC eliminates the current sources and the RC filter found in analog PLLs. The TDC is used to compare the DCO output frequency to a reference frequency. The resolution of the TDC is very important for the performance of the digital PLL because it has a critical effect in causing in-band phase noise. In IEEE 80.15.4g system, the resolution of TDC should be less than 5 ps in order to meet the in-band phase noise of the digital PLL. To improve the frequency resolution and tuning range performance of the digital PLL, the performance of the time-to-digital converter (TDC) and the digitally controlled oscillator (DCO) is most important.

Analog PLL has been frequently used to implement the FSK modulator. The conventional analog PLL is directly modulated by varying the division value of the feedback divider with the output of the additional Σ-Δ modulator [2]. The power consumption is increased,
because additional blocks are needed to implement the FSK modulation. However, because the ADPLL is operated in the digital domain, the modulator can be realized simply.

In this paper, ADPLL is adopted instead of the conventional analog phase-locked loop as a building block for an RF transceiver. In this paper, an FSK modulator with an all-digital PLL is proposed to meet the low power requirements of the IEEE 802.15.4g system.

II. TRANSMITTER ARCHITECTURE

In IEEE 802.15.4g system, the frequency deviations corresponding to ‘1’ and ‘0’ are $+F_{dev}$ and $-F_{dev}$, respectively, where $F_{dev}$ is 25 kHz when mandatory data rate of 50 kb/s is used [1].

Fig. 1 shows the block diagram of the proposed RF FSK transmitter. It is composed of a digital phase-locked loop, power amplifier, LO driver, and FSK modulator. The digital phase-locked loop is composed of a PFD, pulse generator, time to digital converter (TDC), digital filter, DCO (digital controlled oscillator), and dual modulus divider.

The frequency of the reference clock is 24 MHz and the input range of the TDC is 42 ns, which corresponds to one period of the reference clock. The Pulse_A and Pulse_B are outputs of PFD which corresponding to the phase and frequency difference between the reference clock (REF_CLK) and divided DCO clock($F_{DCO\_N}$) are applied to the TDC.

TDC converts the time difference between Pulse_A and Pulse_B into the digital code, $TDC\_O<14:0>$. The channel frequency number is added to the output of TDC and transferred to the Digital Filter. Channel frequency is controlled by adjusting the channel frequency number. The Scale & Mapping block generates the digital control code to a digitally controlled oscillator (DCO). The output frequency of the DCO is divided by a Dual Modulus Divider. Output of the DCO is connected to a power amplifier (PA) to drive the transmitter antenna.

In order to implement the FSK modulator with the all-digital PLL, one of two digital codes corresponding to $+F_{dev}$ and $-F_{dev}$ is selected depending on Tx_Data, and added to the input of DCO to modulate the DCO frequency, and modulated Tx output frequency is calculated by (1) and (2).

When Tx_Data is “1”,

\[
\text{Frequency of } TX\_OUT = (N/2)/((TDC\_Resolution \times TDC\_O) + \text{Channel Frequency}) + F_{dev} \tag{1}
\]

and if Tx_Data is “0”,

\[
\text{Frequency of } TX\_OUT = (N/2)/((TDC\_Resolution \times TDC\_O) - \text{Channel Frequency}) - F_{dev} \tag{2}
\]

where N is the division ratio.

III. BUILDING BLOCKS

A. Time-to-Digital Converter

The quantization noise due to the finite resolution of the TDC, $\Delta T_{RES}$, affects the in-band phase noise of the ADPLL. Therefore, the in-band phase-noise, $L$, at the output of the ADPLL due to the TDC timing quantization can be calculated as (3):

\[
L = 10\log\left(\frac{2\pi}{12} \left(\frac{\Delta T_{RES}}{T_V}\right)^2 \frac{1}{F_{REF}}\right) \tag{3}
\]

where $T_V$ is the DCO clock period and $F_{REF}$ is the reference of the sampling frequency [3].

Fig. 2(a)-(e) shows the block diagram of the proposed three-step TDC.
A three-step time-to-digital converter (TDC) is adopted in order to cover the wide input range of 41.55 ns with the fine resolution of 2.7 ps. The 1\textsuperscript{st} coarse TDC (TDC\textsubscript{1}) in Fig. 2(a) is composed of 15 delay cells with 2.77 ns delay to cover the wide input range of 41.55 ns with 2.77 ns resolution. In order to reduce the variation of TDC output code due to the of PVT variation, the delay compensation scheme is proposed to the delay cell, as shown in Fig. 2(b). The 2\textsuperscript{nd} coarse TDC (TDC\textsubscript{2}) is similar to the 1\textsuperscript{st} coarse TDC, as shown in Fig. 2(c). The 2\textsuperscript{nd} coarse TDC is composed of 31 delay cells with 86.56 ps delay to cover the wide input range of 2.77 ns with 86.56 ps resolution. The time amplifier in Fig. 2(d) amplifies the residue time difference of the 2\textsuperscript{nd} coarse TDC by 5 and transfers it to the fine TDC shown in Fig. 2(e). Thus, the minimum time delay of 86.56 ps in the 2\textsuperscript{nd} coarse TDC is amplified to 393.6 ps by the Time Amplifier.

Time amplifier(TA) amplifies the time difference between two inputs by the TA gain. Thus, when the input time difference is \( T_d \), the output of the time amplifier is \( T_d \times G_{\text{TA}} \) multiplied by the TA gain. Time Amplifier is composed of two latches and delay cells with different delay time.

TA gain is proportional to the capacitance (C) at the output of latch, and inverse proportional to the transconductance (\( g_m \)) of the NAND gate and delay difference (\( \alpha \)) between two latches. In the fine TDC shown in Fig. 2(d), a phase-interpolator is adopted to implement 12.3 ps fine delay from the 98.4 ps delay cell. The total input range and resolution of fine TDC are 393.6 ps and 12.3 ps, respectively.

The block diagram of the proposed TDC architecture with delay compensation is shown in Fig. 3. It consists of reference pulse generator, 1\textsuperscript{st} stage TDC, coarse-tuning block and MUX.

The conventional TDC is very sensitive to the variations of Process, Supply Voltage and Temperature (PVT) since the time delay is changed depending on them [4, 5]. In order to solve the problem, TDC with
delay compensation is proposed and shows the characteristics insensitive to PVT variation.

The operation of the proposed TDC is like this. After the power on, delay compensation function is enabled. During this period, MUX control signal CompSel which is controlled by the coarse-tuning block is set to ‘0’. Then, the input signals of TDC are DN_Comp and UP_Comp which are generated by reference pulse generator. These two signals provide constant time interval to 1st stage TDC. The polarity of UP_Comp is inversion of DN_Comp.

In the case of PVT variations, the output of TDC_1ST_O<8:0> will be changed although TDC input signal is stable. The method of proposed delay compensation block is through changing PVT_CAP<3:0> to correct the deviations. It is controlled by UP/DN_Comp, which is output control signal of coarse tuning block. As a result, time delay of the 1st stage TDC is compensated. Variable time delay is implemented by switching on/off the capacitors between two inverters inside of the delay cell, as shown in Fig. 2(b). In order to guarantee input range of TDC, delay compensation is only applied to 1st stage because the delay of 1st stage is largest. It can be also applied to 2nd and 3rd stage, which would require fine tuning at the post-layout simulation stage to meet the fine resolution.

When the temperature rises up, time delay of the delay cell will be increased, if it is not compensated. In this case, the value of TDC output code would be smaller than that in normal condition. The coarse-tuning block will change the time delay by comparing the TDC code with reference code and adjusting PVT_CAP<3:0> in order to get TDC output of (255)DEC. When delay compensation is finished, Comp_Sel is set to ‘1’. Therefore, F_DCO and F_REF are selected by MUX for TDC input. Normal operation mode of 3-step TDC is turned on with modified PVT_CAP<3:0>.

Timing diagram of the proposed TDC with delay compensation is shown in Fig. 4.

During the normal operation, the output of TDC code, TDC_1ST_O<8:0>, should be “0111111111” in thermometer code ((255)DEC) and this is reference code. When RST is ‘0’, PVT_CAP<3:0> is initialized to “1000” by the coarse-tuning block. After the reset, TDC_1ST_O<8:0> is sensed and compared with reference code by coarse-tuning block.

If the TDC_1ST_O<8:0> is smaller than reference code, Coarse-tuning Down will be HIGH decreasing PVT_CAP<3:0>. On the other hand, if it is larger than reference code, Coarse-tuning UP will be HIGH, increasing PVT_CAP<3:0>. This process will continue until TDC_1ST_O<8:0> is same as reference code. One clock delay is inserted between PVT_CAP<3:0> and TDC_1ST_O<8:0> because the time delay of TDC delay chain should be considered.

Fig. 5 shows the block diagram of the proposed phase-interpolator with resistor tuning array. The phase interpolator generates eight equal phases from the two inputs using the resistor ladder. When time difference between two inputs was told as T_Dc, the outputs of the Phase Interpolator are spaced by T_Dc/8.
B. Digitally Controlled Oscillator

Fig. 6 shows the block diagram of DCO. It is composed of an active inductor, passive inductor, differential MOS varactor, MIM capacitor, and negative-gm cell. A capacitor bank composed of MIM capacitors is designed to cover the wide tuning range by compensating for the PVT variation. The active inductor is used for middle band frequency tuning. The passive inductor is used in parallel with the active inductor in order to minimize the degradation of Q-factor due to the active inductor [6]. As the portion of the active inductor is increased compared with that of the passive inductor, the tuning range is wider and the phase noise performance is degraded since the overall Q-factor is dominated by the active inductor. Thus, the ratio of active inductor and passive inductor is optimized to improve the phase noise and tuning range in this work.

Fig. 7 shows the schematic of the active inductor. It is a differentially configured gyrator-C active inductor.

The total inductance of the active inductor is given by:

$$L_{eq} = 2(C_{p1} + C_{p3} + C_{w1})/G_{ds} (2G_{m1} + G_{m3} - G_{d3})$$  \hspace{1cm} (4)

$$G_{ds} = \lambda I_{ds}$$  \hspace{1cm} (5)

where $C_{wire}$ is the wired capacitance for the tuning bank, and $G_{ds}$ is the drain conductance of $M_{2,9:0}$ in Fig. 7. From (4), the inductance ($L_{eq}$) can be tuned by varying $G_{ds}$. $G_{ds}$ is controlled by $I_{ds}$ from (5). $I_{ds}$ is controlled by the DCONT<9:0> in the active inductor control bank in Fig. 7.

Fig. 8 shows the differential MOS varactor circuit and C-V characteristic graph. The differential MOS varactor is also used for fine frequency tuning. Fine capacitance can be effectively implemented by using the capacitance difference in accumulation mode and inversion mode of the differential MOS varactor [7].

When the oscillation amplitude is $A_{osc}$, the total capacitance ($\Delta C$) is given by:

$$\Delta C = (C_A + C_B) - (C_C + C_D)$$  \hspace{1cm} (6)

where $C_A$ and $C_D$ are capacitances in inversion mode, $C_B$ and $C_C$ are capacitances in accumulation mode.

An input tuning code word, DTW<14:0>, finely controls the frequency of the DCO by adjusting the value of differential MOS varactor. Also, the dithering output (SDM<2:0>) of a second-order sigma-delta modulator (SDM) is applied to the differential MOS varactor in order to increase the resolution of the DCO.

The coarse tuning controller in Fig. 1 selects the
optimum capacitance values, \( \text{CAPS}<9:0> \), to cover the target frequency closely against the PVT variations of the inductor or capacitances. In addition, active inductor control bits, \( \text{DCONT}<9:0> \), adjust the frequency of the DCO by the middle frequency amount between the wide range coarse tuning and fine tuning.

Noise characteristics could be improved by coarse tuning and gain tuning as pre-stage of DCO. But current consumption on negative-gm is rising up because of capacitance increased. Therefore, as frequency decreasing, the output swing of DCO is also decreased.

C. Power Amplifier

Fig. 9 shows the schematic of the power amplifier in the transmitter.

It is composed of four driver amp (DA) Cells. The power gain of DA is controlled digitally. In order to obtain high power gain with small DC current, a class-AB type power amplifier is adopted. A cascode amplifier structure is adopted to guarantee the stability by isolating the input and output under the high output power condition. An inductive load is used to improve the filtering characteristics by configuring the band-pass filter at 915 MHz band.

An on-chip spiral inductor is used as a load. Modeling of the bondwire inductance, PAD capacitance and output matching networks are included in a simulation. Cascode based DA power cells are connected in parallel, and the number of active DA power cells are controlled by a 4-bit control signal, \( \text{DA\_CONT}<3:0> \), in order to control the output power level.

![Fig. 9. Schematic of the power amplifier.](image)

IV. EXPERIMENTAL RESULTS

This chip is implemented in a CMOS 0.18 \( \mu \text{m} \) process. Fig. 10 shows the chip microphotograph. The die area of the full transmitter and ADPLL are 3.5 mm\(^2\) and 1.54 mm\(^2\), respectively.

Fig. 11 shows the measured tuning curve of the DCO. The overall frequency tuning range is 0.364 GHz. The frequency resolution for the 1-LSB of the DTW<14:0> is 684 Hz. The effective time-averaged frequency resolution (\( \Delta f^{\Delta t} \)) done by the 5-bit SDM can be calculated as (7).

\[
\Delta f^{\Delta t} = \frac{684 \text{ Hz}}{2^5} = 21.4 \text{ Hz}
\]  

Thus, the gain of DCO is 21.4 Hz/LSB with SDM.

Fig. 12 shows the simulation result of the three-step TDC. The decimal number output of the three-step TDC when the time difference of Pulse_A and Pulse_B applied to TDC is swept from 0 ns to 42 ns. The gain of

![Fig. 10. The chip microphotograph.](image)

![Fig. 11. The measured tuning curve of the DCO.](image)
TA is designed to be 4.5 in this work. The resolution and input range of the proposed three-step TDC are 2.7 ps and 41.55 ns, respectively.

Figs. 13(a) and (b) show the PVT simulation results of TDC with the delay compensation block. When PVT\_CAP<3:0> is “1000” and the delay compensation block is turned off, the variation of the time delay due to the process variation ranges from -15.9% to +22%, as shown in Fig. 13(a).

On the other hand, when PVT\_CAP<3:0> is “1000” and the delay compensation block is turned on, the 
variation of the time delay due to the process variation is less than \( \pm 1\% \), as shown in Fig. 13(b).

Fig. 14(a) and (b) show the PVT corner simulation result of the TDC output code when the time difference between Pulse B and Pulse_A is 14 ns. In this case, TDC output code should be 5183 without PVT variation. When delay compensation is turned off, TDC output code error ranges from -15.9 % to +22 %, as shown in Fig. 14(a). On the other hand, TDC output code error can be reduced to \( \pm 1\% \) of the nominal value.

As shown in Fig. 15, the measured phase noise is -121.17 dBC/Hz at 1 MHz offset when the DCO output frequency is 1.8 GHz.

Fig. 16 shows the simulation result of the FSK modulation using ADPLL. Before \( t = 10 \mu s \), ADPLL is

![Fig. 12. Simulation result of the three-step TDC.](image)

![Fig. 13. PVT simulation results of TDC with proposed delay compensation block when (a) delay compensation is ‘OFF’, (b) delay compensation is ‘ON’.](image)

![Fig. 14. PVT simulation result of The DC output code when (a) delay compensation is ‘OFF’, (b) delay compensation is ‘ON’.](image)

![Fig. 15. Measured phase noise.](image)
in the lock state. After t=15 \mu s, Tx Output Frequency is modulated as the DCO Input Code is modulated.

Fig. 17 shows the measured spectrum at the baseband output of the receiver when FSK modulation is activated at the transmitter. The frequency deviations from the center frequency are \( +25 \text{ kHz} \) and \( -25 \text{ kHz} \) when the Tx_Data’s are “1” and “0”, respectively. The output power level of the transmitter can be controlled from -1.6 dBm to +12 dBm by the gain control signal, DA_CONT<3:0>.

Table 1 shows the measured performance summary of the transmitter. The output frequency range is from 0.8125 to 1.008 GHz. Power consumptions with the ADPLL are 35.36 mW in the minimum output power mode, and 65.57 mW in the maximum power mode.

Table 2 shows the performance comparison with prior works. The figure of merit (FOM) with the frequency tuning range and TDC frequency resolution for the ADPLL can be calculated using

\[
\text{FOM} = \text{PN}(f_{\text{offset}}) + 20\log\left(\frac{T_{\text{res}}}{f_{\text{o}}}ight) + 20\log\left(\frac{P_{\text{DC}}}{1\text{mW}}\right) - 20\log\left(\frac{\text{FDR}}{10}\right)
\]

where \( f_{\text{offset}} \) is the offset frequency, \( f_{\text{o}} \) is the oscillation frequency, \( \text{PN}(f_{\text{offset}}) \) is the phase noise at \( f_{\text{offset}} \), \( T_{\text{res}} \) is the frequency resolution of TDC, \( P_{\text{DC}} \) is the DC power consumption of the ADPLL, and the FDR is the frequency tuning range as a percentage. The phase noise performance of this work is better than those of [4, 5], and [8].

In addition, the resolution of the TDC is the smallest
except for [4], and the frequency resolution of the DCO is the smallest of all. Also, the proposed ADPLL has the lowest power consumption. From all of the above, FOM is calculated as -386.12 dBe/Hz.

V. CONCLUSIONS

This paper presents a low power FSK (frequency shift keying) transmitter using ADPLL (all digital PLL). In order to operate at low-power and to integrate in a small die area, the ADPLL is adopted in the transmitter. The phase noise of the ADPLL is improved by using a fine resolution TDC (time to digital converter) and DCO (digitally controlled oscillator).

The FSK transmitter is implemented in 0.18 µm 1-poly 6-metal CMOS technology. The die area of the transmitter are 3.5 mm². The total power consumption of the transmitter are 35.36 mW and 65.57 mW when the output power levels are -1.6 dBm and +12 dBm, respectively. The frequency resolution of the TDC is 2.7 ps and the effective DCO frequency resolution with the differential MOS varactor and SDM is 21.4 Hz. The phase noise of the ADPLL output at 1.8 GHz is -121.17 dBe/Hz with a 1 MHz offset.

ACKNOWLEDGMENTS

This work was supported by the IT R&D program of MKE/KEIT [10041864, development on Spectrum Efficient Multiband WPAN System for Smart Home Networks]. This work was also supported by IC Design Education Center(IDEC).

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