Suppression Techniques of Subthreshold Hump Effect for High-Voltage MOSFET

Ki-Ju Baek*, Kee-Yeol Na**, Jeong-Hyeon Park***, and Yeong-Seuk Kim*

Abstract—In this paper, simple but very effective techniques to suppress subthreshold hump effect for high-voltage (HV) complementary metal-oxide-semiconductor (CMOS) technology are presented. Two methods are proposed to suppress subthreshold hump effect using a simple layout modification approach. First, the uniform gate oxide method is based on the concept of an H-shaped gate layout design. Second, the gate work function control method is accomplished by local ion implantation. For our experiments, 0.18 μm 20 V class HV CMOS technology is applied for HV MOSFETs fabrication. From the measurements, both proposed methods are very effective for elimination of the inverse narrow width effect (INWE) as well as the subthreshold hump.

Index Terms—shallow trench isolation (STI), subthreshold hump effect, high-voltage, MOSFET, work function, layout, narrow width effect (NWE), inverse narrow width effect (INWE)

I. INTRODUCTION

Recently, embedding high-voltage (HV) devices into the advanced low-voltage (LV) complementary metal-oxide-semiconductor (CMOS) technology has been an important trend of a cost-effective system on a chip (SoC) solution in the areas of power management integrated circuit, automotive electronics, sensor interface and flat panel display driver applications [1-3]. Shallow trench isolation (STI) is generally used instead of the local oxidation of silicon (LOCOS) because MOSFET has been scaled down to satisfy low power, high speed, and small size requirements for modern applications. STI technology offers a better isolation and larger device density. However, the abrupt transition from the field to an active region in the STI edge significantly influenced the electrical characteristics of HV MOSFETs, resulting in the subthreshold hump effect and inverse narrow width effect (INWE) [4, 5]. The root cause of the subthreshold hump effect is well recognized [6]. The threshold voltage (V_T) at the channel edges is reduced by the enhanced fringing electric field due to field crowding. Another reason for the hump predominantly in the HV n-channel MOSFET (nMOSFET) is the lower surface doping concentration at the channel edges due to the boron. The boron segregation more easily induces the depletion of the channel edge. For this entire mechanism, a parasitic edge transistor with reduced V_T is observed at the channel edge. Therefore, the subthreshold hump can define as a current summation of a parasitic edge transistor and main channel HV MOSFET [7]. As a result, there is an increase in the subthreshold swing and off-state leakage current, which is especially harmful for low power applications. In addition, the subthreshold hump at the negative body bias worsens the functionality of the analog circuit, such as current mismatch in cascode current mirrors [8]. The off-state leakage and device mismatching caused by the subthreshold hump are also limitations of the device scale-down and analog circuit design using small geometry MOSFET [9, 10].
In order to solve the subthreshold hump problem, many solutions have been proposed [11-17]. It is possible to reduce the oxide recess and corner rounding at the STI corner using an additional complicated process [11-16]. A relatively simple approach to eliminate the $V_T$ difference between the parasitic edge transistor and the main channel MOSFET is the large angle tilted ion implantation of specific dopant to the sidewalls of the trench [17]. However, the parameters of the large angle tilted ion implantation must be controlled carefully and additional photolithography is required. Thus, the process of CMOS technologies embedded HV devices would be more complicated and increase the fabrication cost. In addition, the extra process steps required for HV MOSFET can cause the degradation of the electrical characteristics of LV devices. As a result, an alternative solution without any extra fabrication process is desirable. Several simple approaches have been proposed using layout modification. Oishi et al. have proposed an H-shaped gate structure which can successfully suppress the isolation edge effect [5]. However, it needs to be a larger size and is not a suitable structure for HV devices which are more complicated than LV devices. Another method is channel doping control using the baseline p-well [18]. The p-well ion implantation easily compensates for the reduced $V_T$ of parasitic edge transistor in HV devices. This technique is well-known and a commonly used method in HV CMOS technologies. However, relatively high and fixed p-well doping concentration causes large $V_T$ shifts of narrow channel devices. Park et al. proposed another simple method using undoped poly-Si for the elimination of parasitic edge transistors for HV devices [19]. However, this method may not be sufficient to suppress severe subthreshold hump characteristics because the $V_T$ shift of undoped poly-Si is 0.56 V.

In this paper, we describe the characteristics of the subthreshold hump effect of a 0.18 μm 20 V class HV MOSFETs and proposed two suppression techniques for the subthreshold hump using only layout modification without any extra fabrication processes. The first is the uniform gate oxide method (Proposed 1) which is used to eliminate the parasitic edge transistor, whereby the STI divot of the channel edge is located on the outside of the poly-Si gate and the gate oxide thickness of the channel area is to be uniform. The second method is gate work function control using local ion implantation (Proposed 2). In modern CMOS technology, the commonly used gate material is n+ and p+ doped polycrystalline silicon (poly-Si) and the gate work function depends on dopant and doping concentration of ion implantation. Thus, to control gate work function, local ion implantation was applied. Both of techniques are simple and effective to suppress subthreshold hump. In addition, we also present the limitations of each proposed method.

II. DEVICE STRUCTURE AND FABRICATION

A 0.18 μm HV CMOS technology was applied for fabrication. The major features of the HV CMOS technology are a quadruple well (HV n-well, HV p-well, n-well, p-well), dual gate oxide (7 nm, 50 nm), STI, dual gate material (i.e. n+ and p+ doped poly-Si gate) and cobalt salicide (CoSi$_2$) for source and drain.

The major process flow is as follows: HV n-well and p-well formation, STI formation, lightly doped n-drift and p-drift junction ion implantation and drive-in for HV MOSFETs, retrograded n-well and p-well formation for LV MOSFETs, thick gate oxidation (46 nm), selective wet etching to remove oxide for LV device area, thin gate oxidation (7 nm), undoped poly-Si deposition (250 nm), gate patterning, lightly doped drain (LDD) junction formation by ion implantation and SiO$_2$/Si$_3$N$_4$ (15 nm / 55 nm) dielectrics spacer formation, n+ source and drain junction ion implantation (As$^{+}$, 50 keV, and $5\times10^{15}$/cm$^2$), p+ source and drain junction ion implantation (BF$_2$$^{+}$, 20 keV, and $4\times10^{15}$/cm$^2$), CoSi$_2$ formation, Si$_3$N$_4$ capping layer deposition and BPSG for poly-to-metal (PMD) dielectric with chemical mechanical polishing (CMP) planarization, contact, and four levels of metal interconnections with TEOS inter-metal dielectrics with CMP planarization.

A cross sectional view and layout of the fabricated HV nMOSFETs are shown in Fig. 1. The n-drift region of the source and drain sides is lightly doped to endure a breakdown voltage (BV) higher than 25 V. To reduce contact resistance, the poly-Si gate, n+ source, and drain are adopted by the CoSi$_2$. The minimum channel length and width of the test structure are 1.6 μm and 1.0 μm, respectively.
In this section, we will describe the characteristics of the subthreshold hump effect of the fabricated HV nMOSFETs in applied HV CMOS technology and propose two suppression techniques of subthreshold hump using only layout modification without any extra fabrication processes.

1. I-V Characteristics at Subthreshold Regime

Fig. 2 shows the measured drain current versus gate voltage ($I_D$-$V_{GS}$) characteristics of HV nMOSFET which were measured at different negative body voltages ($V_{BS}$). The channel length ($L$) and width ($W$) of the test structure are 3.6 μm and 10.0 μm, respectively. The drain voltage ($V_{DS}$) is applied for 0.1 V. As $V_{BS}$ increases in the negative direction, the hump strength of HV nMOSFET increases due to the reduced sensitivity of the parasitic edge transistor to the body bias compared with the main channel MOSFET. It is well known that the body coefficient is a function of the body doping concentration and the gate oxide capacitance. The transistor becomes less sensitive to the body bias if the body doping concentration is lower or the gate oxide capacitance is higher due to oxide recess. Thus, the $V_T$ difference between the parasitic edge transistor and the main channel MOSFET increases with the negative body bias.

Fig. 3 shows the measured $V_T$ of HV MOSFETs on the channel width variation. The channel widths of test structures range from 1.0 to 10.0 μm. The $V_T$ of the HV nMOSFETs reduces as the channel width decreases; thus the INWE are shown in Fig. 3. The $V_T$ difference between the wide and narrow channels of HV nMOSFET is 80 mV. The narrow channel device shows stronger electrical characteristics of the parasitic edge transistor and the drain current of the narrow channel device is dominated by the parasitic edge transistor. For the wide channel device, the drain current of the parasitic edge transistor can be neglected.

Fig. 4 shows transmission electron microscopy (TEM) image of the fabricated HV nMOSFET. The TEM micrograph shows a cross sectional view around the STI corner. The upper active corner rounding is reasonable...
but the gate oxide thinning is clearly shown at the channel edge. The gate oxide thickness at the channel edge is about 46 nm, while the thickness of gate oxide at the channel center is 50 nm. The gate oxide thinning is one of the root causes of the subthreshold hump effect. Since the doping concentration at the surface of HV nMOSFET is considerably low for high junction BV, the boron segregation more easily induces depletion of the channel due to field crowding. Boron segregation at the STI edges is another root cause of subthreshold hump of HV nMOSFET. Thus the fabricated HV nMOSFETs have both subthreshold hump effect and INWE.

2. Proposed Suppression Methods of Subthreshold Hump

This section describes our approach to solving the subthreshold hump issue in the applied HV CMOS technology. Both of the proposed methods are limited to layout modification. Thus, no additional lithography or special processing steps are required in the applied fabrication process.

Fig. 5 shows proposed layouts to prevent parasitic edge transistor turn-on. Fig. 5(a) shows the test structure of the uniform gate oxide method (Proposed 1). To eliminate the parasitic edge transistor, the active layer of test structures is designed to enclose the poly-Si gate. Thus, the STI divot of the channel edge is located outside the poly-Si gate and the gate oxide thickness of the channel edge is identical to that of the channel center area. The uniform gate oxide thickness is helpful to obtain better gate oxide reliability and there is also no boron segregation at channel edge. Fig. 5(b) shows the test structure of the gate work function control using local ion implantation (Proposed 2). In modern CMOS technology, n+ or p+ doped poly-Si by ion implantation is used as the gate material and the gate work function depends on its dopant and doping concentration. The nMOSFET with p+ doped poly-Si gate has higher \( V_T \) than the nMOSFET with n+ doped poly-Si gate due to flat band voltage difference. If the parasitic edge transistor has higher \( V_T \) than the main channel MOSFET, the channel of the parasitic edge transistor cannot easily be depleted and subthreshold hump can be suppressed. Thus, to control the gate work function of the parasitic edge transistor, selective p+ ion implantation was applied for the gate end cap and poly-Si gate located at the channel edge. The gate end cap of the poly-Si gate (\( L_E \)) is 0.3 \( \mu \)m. The overlap length of the p+ doped poly-Si gate and silicon active layer (\( L_O \)) is 0.3 \( \mu \)m at each channel edge to prevent lithography misalignment. The baseline n+ and p+ source/drain ion implantations were used for the n+ and p+ doped poly-Si, respectively. Both p+ and n+ poly-Si are connected electrically through a CoSi\(_2\) layer. The measured \( V_T \) of HV nMOSFET with the n+ and p+ poly-Si are 0.96 V and 1.97 V, respectively.
The measured $I_D$-$V_{GS}$ characteristics of HV nMOSFETs for the conventional and proposed methods are shown in Fig. 6. The conventional method [18] and our two proposed methods can suppress subthreshold hump effectively. However, the conventional method [19] is not sufficient to suppress subthreshold hump at a large negative body voltage.

Fig. 7 shows the measured $V_T$ of the conventional and proposed methods as a function of the channel width. The INWE is shown in both the reference and conventional method [19]. However, there is no $V_T$ change regardless of the channel width for the proposed method 1. But, the conventional method [18] and the proposed method 2 show the narrow width effect (NWE) like MOSFET with LOCOS isolation. The $V_T$ of the conventional method [18] increases abruptly as the channel width decreases because of relatively high surface doping concentration and lateral diffusion of p-well in the narrow channel device. On the other hand, the proposed method 2 has no lateral diffusion and the 0.3 μm overlap length only affect $V_T$ increase. Therefore, $V_T$ shift is small compared to the conventional method [18].

Fig. 8 shows the measured $V_T$ of the conventional and proposed methods as a function of the channel length. The channel lengths of the test structures are from 1.6 to 9.6 μm, and $W$ is identical to 10.0 μm. The $V_{BS}$ are applied at 0 V and -5 V. The short channel effect (SCE) is shown in all devices. However, smaller $V_T$ reduction as $L$ decreases is shown in all applied methods compare to the reference device. The INWE of the reference device results in a more severe SCE. These characteristics are shown more apparently at a large body voltage ($V_{BS}$ = -5 V). Suppression of subthreshold hump can also help suppress the SCE and well described in the previous study as the mixing effect [5].

Fig. 9 shows the measured drain saturation current...
Table 1. Advantage and disadvantage of the proposed techniques

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<tr>
<th>Techniques</th>
<th>Advantages</th>
<th>Disadvantages</th>
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<tr>
<td>[18] Channel doping control by p-well ion implantation</td>
<td>- Simple and cost effective</td>
<td>- High $V_T$ shift of narrow width devices - BV lowering by lateral diffusion of p-well</td>
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<tr>
<td>[19] Gate work function control by undoped poly-Si</td>
<td>- Simple and cost effective</td>
<td>- Imperfect suppression of severe hump</td>
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<tr>
<td>Proposed 1 Uniform gate oxide</td>
<td>- Simple and cost effective - Good gate oxide reliability</td>
<td>- High $I_D$ shift of narrow width devices</td>
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<tr>
<td>Proposed 2 Gate work function control by p+ poly-Si</td>
<td>- Simple and cost effective</td>
<td>- Strict photo-alignment control</td>
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Fig. 10. BV characteristics of the fabricated HV nMOSFETs for conventional and proposed methods ($V_{GS} = V_{BS} = 0$ V).

(ID$_{SAT}$) of the conventional and proposed methods as a function of the channel width. The $V_{DS}$ and $V_{GS}$ are applied at the same 20 V. $I_{D,SAT}$ of the proposed method 1 increases abruptly as $W$ decreases. Such enhancement of $I_{D,SAT}$ is due to additional channel width that is formed by the n-drift layers and extension of the active layer. The total $W$ of the minimum narrow channel device using the proposed method 1 changes from 1.0 μm to 1.6 μm. As a result, $I_{D,SAT}$ of the narrow channel device is increased by 55%. HV MOSFETs are usually used with very large $W$. If narrower channel device using the proposed method 1 is employed for circuit design, $W$ enhancement must be compensated.

Fig. 10 shows the measured off-state BV characteristics. The geometry of the measured devices is a minimum size. The channel length and width are 1.6 μm and 1.0 μm, respectively. The $V_{GS}$ and $V_{BS}$ are applied at the same 0 V. All of the applied suppression methods can help reduce off-state leakage current at $V_{DS} = 20$ V. The BV of the conventional method [18] is 26 V and approximately 0.8 V lower than that of other methods. The 0.8 V BV lowering is not critical in the applied technology for fabrication. However, large BV reduction of short and narrow channel devices using the conventional method [19] is frequently observed due to high surface doping concentration and lateral diffusion of p-well. The conventional method [19] results in a limitation of device scale-down.

As discussed previously, both of the proposed techniques are effective to suppress subthreshold hump effect. Even though both of the proposed techniques have limitations, these techniques are very simple and still applicable. The advantages and disadvantages of the proposed techniques are summarized in Table 1.

V. CONCLUSIONS

We have proposed two simple and effective methods for suppression of hump effect in a subthreshold regime. Both of the simple techniques used layout modification. Even though both proposed techniques have disadvantages, these techniques eliminate the subthreshold hump successfully. Obviously, elimination of the subthreshold hump can reduce standby leakage currents and power consumption as well as subthreshold current matching. We expect that these techniques are very effective methods for suppressing hump effect for HV devices.

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REFERENCES


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