Dependence of the 1/f Noise Characteristics of CMOSFETs on Body Bias in Sub-threshold and Strong Inversion Regions


Abstract—In this paper, the 1/f noise characteristics of n-channel MOSFET (NMOSFET) and p-channel MOSFET (PMOSFET) are analyzed in depth as a function of body bias. The normalized drain current noise, $S_{ID}/I_D^2$, showed strong dependence on the body bias in the sub-threshold region for both NMOSFET and PMOSFET, and NMOSFET showed stronger dependence than PMOSFET on the body bias. On the contrary, both of NMOSFET and PMOSFET do not exhibit the dependence of $S_{ID}/I_D^2$ on body bias in strong inversion region, although the noise mechanisms of two MOSFETs are different from each other.

Index Terms—CMOSFET, 1/f noise, NMOSFET, PMOSFET, body bias, sub-threshold region

I. INTRODUCTION

Low frequency noise has become one of the major issues for analog/mixed signal and radio frequency (RF) circuits [1-4]. This is mainly due to the improvement of device performance by the continuous scaling down of the gate length of the metal oxide semiconductor field effect transistors (MOSFETs). Recently, the demand for low power consumption has increased due to the development of single battery mobile appliances. Therefore, to reduce the dynamic power consumption of complementary metal oxide semiconductor (CMOS) circuits the threshold voltage must be scaled down along with the supply voltage without degrading the circuit speed or the operating logic noise margins. Although the threshold voltage scaling is limited by the off-current and static power consumption constraints, a constant substrate biasing technique is used with standard CMOS technology to improve the performance of CMOS circuits [5]. Forward biasing the substrate reduces the threshold voltage of the MOSFET and increases the speed of the device in analog/mixed signal CMOS circuits. Reverse body biasing is attractive for low current CMOS applications as the device’s active mode current decreases, and this means the signals become comparable with the low frequency noise (LFN) [6]. As this technique can be used in analog integrated circuits such as the current mirror and voltage controlled oscillator (VCO), the dependence of 1/f noise characteristics on body bias needs to be analyzed. However, there are few reports on the analysis of noise characteristics considering the body biases in the sub-threshold and strong inversion regions [7, 8].

Previous experiment showed 1/f noise characteristics with various body bias in sub-threshold region [9]. However, it showed NMOSFET’s characteristics only and the analysis was not quite clear. Thus, in this study, the 1/f noise characteristics of both NMOSFETs and PMOSFETs were investigated concurrently and
systematically for various body biases from the sub-threshold to strong inversion regions. Moreover, the noise characteristics were analyzed as a function of drain current with a variable of body bias for both NMOSFET and PMOSFET.

II. EXPERIMENTAL DETAILS

Conventional NMOSFET and PMOSFET with a gate width of 20 µm and length of 0.13 µm were used for the analysis of the low frequency noise (LFN) characteristics. The LFN measurements were performed in a shielded probe station. The device under test (DUT) was biased using an HP 4156C Parameter analyzer and the drain current noise was amplified with an SR 570 low noise current amplifier. The apparatus configuration is schematically shown in Fig. 1. The drain current noise power spectral density (PSD), $S_{id}$, was measured using an HP 35670A dynamic signal analyzer in the frequency range of 1 Hz to 12.8 kHz. The DC characteristics of both NMOSFET and PMOSFET were measured prior to 1/f noise measurements. To observe the body bias dependence of 1/f noise, the constant body bias in the range of +0.5 V to −0.75 V for NMOSFETs and −0.5 V to +1 V for PMOSFETs was applied to the substrate during the LFN measurements.

III. RESULTS AND DISCUSSION

Figs. 2(a) and (b) show the DC characteristics of NMOSFET and PMOSFET with a body bias variable. The depletion width increases under the reverse body bias and decreases under the forward body bias due to the change of potential difference between the source and the body junction. The depletion charge is expressed by

$$Q_D = \varepsilon N_{sub} X_d = \sqrt{2 \varepsilon_\text{Si} N_{sub} (2|\varphi_0| + V_{BS})} \quad (1)$$

where $N_{sub}$ is the body doping density, $X_d$ is the depletion width, $\varepsilon_\text{Si}$ is the dielectric constant for silicon, $\varphi_0$ is the flat band potential, and $V_{BS}$ is the applied body bias. Under reverse body biasing, the drain saturation current decreases due to the increased threshold voltage. The forward body biasing causes the decrease of depletion.
charges and results in a decrease of the threshold voltage and an increase of the drain saturation current.

Figs. 3(a) and (b) shows the typical flicker noise shape of NMOSFET and PMOSFET under zero body bias. The drain current noise power spectral density level of NMOSFET and PMOSFET are increased with increasing gate bias as well known.

Fig. 4(a) shows the variation of the normalized drain current noise power spectral density, \( S_{\text{ID}}/I_D^2 \) against the drain current \( I_D \) with the various body biases for NMOSFET. The normalized drain current noise shows similar trend with the square of the normalized transconductance \( (g_m/I_D)^2 \) in the strong inversion region, which implies the carrier number fluctuations [10].

When the gate voltage is below the threshold voltage, the surface is in weak inversion and the current flow is dominated by diffusion. The normalized flicker noise expression [11] in weak inversion is given below,

\[
\frac{S_{\text{ID}}}{I_D^2} = \frac{q^4 \lambda N_t}{kTWLf(C_{ox} + C_D + C_a)^2} \tag{2}
\]

where \( \lambda \) is the tunnel attenuation distance of the electron and hole in the oxide (\( \lambda \) is 0.1 nm), \( N_t \) is the oxide trap density, \( k \) is the Boltzman’s constant, \( T \) is the absolute temperature, \( W \) and \( L \) are the width and the length of the channel, and \( C_{ox}, C_D, \) and \( C_a \) are the oxide, depletion, and
From the equation, it can be seen that the normalized flicker noise is dependent on the depletion capacitance and the depletion capacitance is \( V_{\text{BS}} \) dependent. The depletion capacitance decreases with increasing reverse body bias and it causes increase of the normalized drain current in weak inversion region.

Fig. 5 shows the normalized drain current noise power spectral density of NMSOFET and PMOSFET as a function of body bias. As we can see in Figs. 5(a) and (b), the normalized drain current noise PSD increases with the increased reverse body bias in the sub-threshold region, mainly due to the decrease of the depletion capacitance (\( C_D \)) in both NMSOFET and PMOSFET.

As the reverse body bias increasing, the depletion region is increased for both NMOSFET and PMOSFET. Enlarged depletion area with reverse body bias results in decrease of the depletion capacitance. However, there is not much difference in the strong inversion region, and this can be explained by considering the charge conservation principle [6]. The variation of the inversion charge \( \delta Q_{\text{inv}} \) is given by

\[
\delta Q_{\text{inv}} = \frac{-C_{\text{inv}}}{C_{\text{ox}} + C_D + C_{\text{it}} - C_{\text{inv}}} \delta Q_{\text{ox}}
\]

where \( C_{\text{inv}} \), \( C_{\text{ox}} \), \( C_D \) and \( C_{\text{it}} \) are the inversion, oxide, depletion and interface charge capacitance per unit area respectively. Assuming that \( C_{\text{inv}} \gg C_{\text{ox}} + C_D + C_{\text{it}} \) in the strong inversion region, the variation of the inversion charge is the same as the fluctuation of the oxide trapped charge that is, \( \delta Q_{\text{inv}} \approx \delta Q_{\text{ox}} \). Thus, the depletion layer becomes negligible in this region and the noise level will not be affected by the body bias \( V_{\text{BS}} \). From that the normalized drain current noise PSD varies less in strong inversion region than that of in sub-threshold region with body bias.

IV. CONCLUSIONS

The dependence of the flicker noise characteristics of NMOSFET and PMOSFET from the sub-threshold region to strong inversion region has been investigated. NMOSFET follows the number fluctuation mechanism and in case of PMOSFET the mobility fluctuation mechanism dominates the flicker noise. The normalized drain current noise level increased as the reverse body bias increased in the sub-threshold region due to the decrease of the depletion capacitance for both NMOSFET and PMOSFET. On the contrary, both MOSFETs do not affected by the applied body bias in strong inversion region. This additional study of flicker noise characteristics from the sub-threshold to strong inversion region with various body biases is worthwhile, especially for the low power application of the CMOSFETs.

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REFERENCES


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