$V_T$-Modulation of Planar Tunnel Field-Effect Transistors with Ground-Plane under Ultrathin Body and Bottom Oxide

Min-Chul Sun$^1$, Hyun Woo Kim$^2$, Hyungjin Kim$^3$, Sang Wan Kim$^2$, Garam Kim$^2$, Jong-Ho Lee$^2$, Hyungcheol Shin$^2$, and Byung-Gook Park$^2$

Abstract—Control of threshold voltage ($V_T$) by ground-plane (GP) technique for planar tunnel field-effect transistor (TFET) is studied for the first time using TCAD simulation method. Although GP technique appears to be similarly useful for the TFET as for the metal-oxide-semiconductor field-effect transistor (MOSFET), some unique behaviors such as the small controllability under weak ground doping and dependence on the dopant polarity are also observed. For $V_T$-modulation larger than 100 mV, heavy ground doping over $1 \times 10^{20}$ cm$^{-3}$ or back biasing scheme is preferred in case of TFETs. Polarity dependence is explained with a mechanism similar to the punch-through of MOSFETs. In spite of some minor differences, this result shows that both MOSFETs and TFETs can share common $V_T$-control scheme when these devices are co-integrated.

Index Terms—Threshold voltage, Tunnel field-effect Transistor (TFET), ground-plane, ultrathin body and bottom oxide (UTBB), TCAD simulation

I. INTRODUCTION

Recently various tunneling-injection floating-body devices, so called tunnel field-effect transistors (TFETs), have been massively studied as a single device due to the extraordinary subthreshold characteristics and capability of low-voltage operation [1-4]. However, there is a lack of studies on practical $V_T$-control schemes compatible with existing low power circuit design techniques [5, 6]. Although a device design with the $V_T$-control doping region was recently proposed from this perspective, needs of asymmetric angled doping process and restriction in the direction of gate lines can limit the practical usefulness [7].

A similar problem in a fully-depleted silicon-on-insulator metal-oxide-semiconductor field-effect transistor (FDSOI-MOSFET) is studied with the ground-plane (GP) or back-gate technique proposed by Xiong et al. (Fig. 1) [8]. Recently this scheme was successfully demonstrated to implement multi-$V_T$ options for metal-gate/high- MOSFETs using ultrathin body and bottom oxide (UTBB) SOI substrate [9].

In this work, we verify the extendibility of GP

![Fig. 1. $V_T$-control schemes of (a) bulk device, (b) ultra-thin-body silicon-on-insulator (UTB-SOI) device, (c) ultra-thin-body-and-box silicon-on-insulator (UTBB-SOI) device.](image-url)
II. Model Device and Definition of Parameters

Fig. 2 and Table 1 summarize the model structure used in this study. Based on the recent studies on UTBB-SOI MOSFETs, the baseline device is defined with 6 nm of SOI and 10 nm of BOX with the raised source/drain [9, 11]. To maximize the current drivability, the source junction is designed within a narrow bandgap material [12]. The drain-side sidewall is formed thicker than the other to suppress the unwanted drain-side tunneling current at off-state.

Fig. 3 shows the typical transfer characteristics of the model device with $V_{DS} = 1$ V. Since the definitions of $V_T$ for the MOSFET based on the strong inversion of the channel are not applicable to TFET, the simple constant current method with a threshold current $I_T$ of 0.1 A/µm is used to define $V_T$. Change in the energy band diagram at the defined $V_T$ is shown in Fig. 4. As for subthreshold swing (SS), the slope of $I_D-V_{DS}$ curve in Fig. 3 continuously changes below $V_T$ unlike those of MOSFETs. This is because the subthreshold current of a TFET is governed by the band-to-band tunneling mechanism, not by the statistical diffusion. Therefore, the SS is defined as the average swing between $V_T$ and $V_D = 0.3 \times V_{DD}$. Calculating the average SS within a fixed interval makes it possible to compare the steepnesses of different subthreshold curves regardless of the $V_D$-s. The value of $0.3 \times V_{DD}$ is used because the $V_D$-s of MOSFETs in logic CMOS technology have been scaled to be

![Fig. 2. Structure of model device: The doped substrate region under bottom oxide acts as the GP layer.](image)

**Table 1. Parameters of baseline device**

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length</td>
<td>24 nm</td>
</tr>
<tr>
<td>Gate oxide thickness ($T_{ox}$)</td>
<td>1 nm</td>
</tr>
<tr>
<td>SOI thickness</td>
<td>6 nm</td>
</tr>
<tr>
<td>BOX thickness ($T_{box}$)</td>
<td>10 nm</td>
</tr>
<tr>
<td>Left-sidewall length</td>
<td>4 nm</td>
</tr>
<tr>
<td>Right-sidewall length</td>
<td>8 nm</td>
</tr>
<tr>
<td>Thickness of raised S/D</td>
<td>15 nm</td>
</tr>
<tr>
<td>n-type Ge thickness</td>
<td>3 nm</td>
</tr>
<tr>
<td>p-type Ge doping</td>
<td>$1 \times 10^{20}$ cm$^{-3}$</td>
</tr>
<tr>
<td>n-type Ge doping</td>
<td>$1 \times 10^{21}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Doping of SOI</td>
<td>$1 \times 10^{18}$ cm$^{-3}$</td>
</tr>
<tr>
<td>n-type Si doping</td>
<td>$1 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Gate work function</td>
<td>4.61 eV</td>
</tr>
</tbody>
</table>

![Fig. 3. Definitions of threshold voltage ($V_T$) and subthreshold swing (SS) in this study: Here $V_T$ is defined by the threshold current method with $I_T = 0.1$ μA/µm. Here $V_{DS} = 1$ V.](image)

![Fig. 4. Energy band diagrams and band-to-band tunneling rate at 0.5 nm below the gate oxide with (a) $V_G = 0$ V, (b) $V_G = V_T$. Here $V_{DS} = 1$ V.](image)
approximately this value in order to keep both a large drive-current and small off-current.

III. Results and Discussion

First, the \( V_T \)-modulation of the baseline device and that of MOSFET are compared with variation of the GP doping from \( 1 \times 10^{14} \) to \( 1 \times 10^{21} \) cm\(^{-3} \) with \( V_{DS} = 1 \) V (Fig. 5). The smaller modulation under light doping conditions and with thicker BOX designs is attributed to higher field-sensitivity of the carrier injection of TFET devices. It also shows that the GP technique for the FDSOI-MOSFET is similarly useful for TFETs if heavy GP doping is used.

Next, the asymmetric sensitivity to the polarity of GP doping is investigated using energy band contours in Fig. 6. While p-type GP blocks the field penetration from the drain and influences on the potential at the tunneling point, n-type GP lets the drain field into the channel region and loses its controllability over the potential at the point. Therefore, p-type doping modulates \( V_T \) more efficiently than n-type does. Meanwhile, since the \( SS \) in this work is defined as the average swing between \( V_T \) and \( V_T - 0.3 \times V_{DD} \) and the change of GP doping does not mean the change of doping in the SOI region, the \( SS \) remains unchanged regardless of the GP doping (Fig. 7).

Finally, the effectiveness of GP technique in the devices with a change of gate dielectric is studied in Figs. 8 and 9. Although smaller \( T_{gox} \) helps to reduce \( V_T \), it also narrows down the window within which GP doping can modulate \( V_T \). As the BOX gets thinner, GP doping exerts more influence over \( V_T \) to the contrary. These are understood from the simple capacitance network model described in Fig. 10. Since the potential at the tunneling point is determined by the capacitive coupling ratios in the network, tighter coupling to the top gate potential leads to reduced modulation window with GP. The
degradation of $SS$ in Fig. 9 can be similarly explained. In the case of n-type GP-doping, the change in $SS$ with BOX thickness is insignificant because the field from the drain weakens the coupling of potentials between GP doping region and the tunneling point.

### III. CONCLUSIONS

We confirmed that the ground-plane technique for the UTBB-SOI MOSFET device is extendible to TFETs. Due to higher sensitivity to electric field, the effectiveness of GP doping in TFET was relatively smaller than that in MOSFET. P-type GP doping blocks the field from the drain only to increase the $V_T$. Since the capacitive coupling effect can degrade $SS$, a compromise between $V_T$-modulation window and $SS$ degradation is needed. This is practically important in that both MOSFET and TFET can share common $V_T$-control scheme when these devices are co-integrated.

### ACKNOWLEDGMENTS

This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186).

### REFERENCES


Min-Chul Sun received the B.S. and M.S. degrees in 1996 and 2001 from Yonsei University and Korea Advanced Institute of Science and Technology respectively. He has been working for the Semiconductor Business Unit of Samsung Electronics Co. Ltd. since then. He received Ph.D. degree in electrical engineering from Seoul National University studying toward the Ph.D. degree in 2013. He participated in the IBM-Samsung Joint Development Project at the IBM Semiconductor Research and Development Center (IBM SRDC, NY) as Front-End-Of-Line integrator for 65- and 45-nm technologies. His current research interests include the ultra-low-power multi-channel transistors, CMOS-compatible nanoelectronics, hybrid channel devices and advanced junction technology with the consideration of circuit design. Mr. Sun is a Student Member of the Institute of Electrical and Electronics Engineers (IEEE) and the Institute of Electronics Engineers of Korea (IEEK).

Hyun Woo Kim received the B.S degrees in 2008 from Kyungpook National University (KNU), Daegu, Korea and he is currently working toward the M.S. degree in Electrical Engineering at Seoul National University (SNU). His research interest is Tunnel FET with nickel silicide.
Hyungjin Kim received the B.S. degree in Electrical Engineering from Seoul National University in 2010. He is currently working toward M.S degree at the department of electrical engineering, Seoul National University, Seoul, Korea. His research interests include nanoscale silicon devices, tunnel field-effect transistor (TFET), and Si-based neuromorphic system.

Sang Wan Kim received the B.S. and M.S. degrees in 2006 and 2008 from Seoul National University (SNU), Seoul, Korea, where he is currently working toward the Ph.D. degree in electrical engineering. His current research interests include 1T DRAM and CNT based device fabrication, characterization, measurement, and modeling. Mr. Kim is currently a Student Member of the Institute of Electronics Engineers of Korea (IEEE).

Garam Kim received the B.S. degree in 2008 from Seoul National University (SNU), Seoul, Korea, where he is currently working toward the Ph.D. degree in electrical engineering. His current research interests include 1-Transistor DRAM fabrication, characterization, measurement, and modeling. Mr. Kim is currently a Student Member of the Institute of Electronics Engineers of Korea (IEEE).

Jong-Ho Lee received the B.S. degree from Kyungpook National University, Daegu, Korea, in 1987 and the M.S. and Ph.D. degrees from Seoul National University, Seoul, in 1989 and 1993, respectively, all in electronic engineering. In 1993, he worked on advanced BiCMOS process development at ISRC, Seoul National University as an Engineer. In 1994, he was with the School of Electrical Engineering, Wonkwang, University Iksan, Chonpuk, Korea. In 2002, he moved to Kyungpook National University, Daegu Korea, as a Professor of the School of Electrical Engineering and Computer Science. Since September 2009, he has been a Professor in the Department of Electrical Engineering and Computer Science, Seoul National University, Seoul Korea. From 1994 to 1998, he was with ETRI as an invited member of technical staff, where he worked on deep submicron SOI devices, device isolation, 1/f noise, and device mismatch characterization. From August 1998 to July 1999, he was with Massachusetts Institute of Technology, Cambridge, as a postdoctoral fellow, where he was engaged in the research on sub-100 nm double-gate CMOS devices. He has authored or coauthored more than 120 papers published in refereed journals and over 220 conference papers related to his research and has been granted 65 patents in this area. His research interests include sub-100 nm device technologies, non-volatile memory devices, device characterization and DC/RF device modeling, device characterization, thin film transistors, and integrated Microsystems including various sensors. Prof. Lee is a Lifetime Member of the Institute of Electronics Engineers of Korea (IEEE). He received several best paper awards from international and domestic conferences, and also received several research awards for excellent research. In 2006, he was a recipient of the “This Month’s Scientist Award” for his contribution in the development of practical high-density/high-performance 3-dimensional nano-scale CMOS devices. He invented Saddle FinFET (or recess FinFET) for DRAM cell and NAND flash cell string with virtual source/drain, which have been applying for mass production, and made a big contribution in memory technology. He has served as a committee member of the International Electron Devices Meeting.
Hyungcheol Shin received the B.S. (magna cum laude) and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from the University of California Berkeley, Berkeley, in 1993. From 1994 to 1996, he was a Senior Device Engineer with Motorola Advanced Custom Technologies. In 1996, he was with the Department of Electrical Engineering and Computer Sciences, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. During his sabbatical leave from 2001 to 2002, he was a Staff Scientist with Berkana Wireless Inc., San Jose, CA, where he was in charge of complementary metal–oxide–semiconductor radio-frequency (CMOS RF) modeling. Since 2003, he has been with the Department of Electrical Engineering and Computer Science, Seoul National University. He is the author of over 450 technical papers in international journals and conference proceedings. He also wrote a chapter in a Japanese book on plasma charging damage and semiconductor device physics. His current research interests include Flash memory devices, dynamic random access memory cell transistors, nanoscale CMOS, CMOS RF, and noise. Dr. Shin is a lifetime member of the Institute of Electronics Engineers of Korea (IEEK). He was a committee member of the International Electron Devices Meeting. He was also a committee member of the IEEE Electron Devices Society Graduate Student Fellowship and of several international conferences, including the International Workshop on Compact Modeling and the Structures, Solid State Devices and Materials. He received the Second Best Paper Award from the American Vacuum Society in 1991; the Excellent Teaching Award from the Department of Electrical Engineering and Computer Sciences, KAIST, in 1998; the Haedong Paper Award from IEEK in 1999; and the Excellent Teaching Award from Seoul National University in 2005, 2007, and 2009. He is listed in Who’s Who in the World.

Byung-Gook Park received his B.S. and M.S. degrees in Electronics Engineering from Seoul National University (SNU) in 1982 and 1984, respectively, and his Ph.D. degree in Electrical Engineering from Stanford University in 1990. From 1990 to 1993, he worked at the AT&T Bell Laboratories, where he contributed to the development of 0.1 micron CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, developing 0.25 micron CMOS. In 1994, he joined SNU as an assistant professor in the Department of Electrical Engineering and Computer Science, where he is currently a professor. In 2002, he worked at Stanford University as a visiting professor, on his sabbatical leave from SNU. He led the Inter-university Semiconductor Research Center (ISRC) at SNU as the director from June 2008 to 2010. His current research interests include the design and fabrication of nanoscale CMOS, flash memories, silicon quantum devices and organic thin film transistors. He has authored and co-authored over 800 research papers in journals and conferences, and currently holds 53 Korean and 22 U.S. patents. He has served as a committee member on several international conferences, including Microprocesses and Nanotechnology, IEEE International Electron Devices Meeting, International Conference on Solid State Devices and Materials, and IEEE Silicon Nanoelectronics Workshop (technical program chair in 2005, general chair in 2007). He is currently serving as an executive director of Institute of Electronics Engineers of Korea (IEEK) and the board member of IEEE Seoul Section. He received “Best Teacher” Award from the department in 1997, Doyeon Award for Creative Research from ISRC in 2003, Educational Award from College of Engineering, SNU, in 2006, and Haedong Research Award from IEEK in 2008.