A CMOS Envelope Tracking Power Amplifier for LTE Mobile Applications

Junghyun Ham¹, Haeryun Jung¹, Hyungchul Kim¹, Wonseob Lim¹, Deukhyoun Heo², and Youngoo Yang¹

Abstract—This paper presents an envelope tracking power amplifier using a standard CMOS process for the 3GPP long-term evolution transmitters. An efficiency of the CMOS power amplifier for the modulated signals can be improved using a highly efficient and wideband CMOS bias modulator. The CMOS PA is based on a two-stage differential common-source structure for high gain and large voltage swing. The bias modulator is based on a hybrid buck converter which consists of a linear stage and a switching stage. The dynamic load condition according to the envelope signal level is taken into account for the bias modulator design. By applying the bias modulator to the power amplifier, an overall efficiency of 41.7 % was achieved at an output power of 24 dBm using the 16-QAM uplink LTE signal. It is 5.3 % points higher than that of the power amplifier alone at the same output power and linearity.

Index Terms—Envelope tracking, power amplifier, CMOS power amplifier, bias modulator, hybrid buck converter, long term evolution

I. INTRODUCTION

Wireless communication systems have evolved with more complex modulation techniques and wider signal bandwidth for higher data rate. For the modulated signals that have high peak-to-average ratio (PAPR) and wide signal bandwidth, power amplifiers (PAs) are required to operate on an output power back-off condition and to comply with very stringent linearity specification. Such a back-off operation in output power level significantly degrades efficiency of the PA. Various techniques have been studied to mitigate this efficiency degradation problem [1-22].

Among several techniques, the envelope tracking (ET) technique has been in great interest due to its high efficiency and moderate linearity characteristics. A block diagram of the ET PA is shown in Fig. 1(a). Basically, ET PA consists of a PA and a bias modulator. The bias modulator dynamically supplies the bias voltage to the PA according to the envelope signal. Then, high efficiency can be maintained even at significantly back-off output power levels from the peak power level, as shown in Fig. 1(b).

Several bias modulators have been proposed for the ET techniques. Low drop-out regulators and switching regulators are not good choice for the bias modulator due to low efficiency and narrow bandwidth, respectively [3, 4]. The hybrid bias modulators, which have a highly efficient switching stage and a broadband linear stage, have been popular for the ET applications [6-22]. The switching stage supplies most of the current which are around very low frequency including DC. The linear stage supplies rest of the current to the PA as a drain bias. The linear stage also compensates for the ripple current from the switching stage.

Because of high efficiency and high power density characteristics, compound processes, such as GaAs HBT
or SiGe BiCMOS, have been dominantly used to design PAs for wireless communication applications. Therefore, the bias modulators, which are generally designed using CMOS process, have been generally applied to those PAs using GaAs HBT or SiGe BiCMOS processes for higher performance [13-20]. However, the PAs based on CMOS process has great advantages in lower cost and higher integration in spite of its relatively poor performances [23-25].

In this paper, both PA and bias modulator are designed and implemented using a standard 0.18-μm CMOS process. The PA has a two-stage differential common-source structure for obtaining sufficient gain and applying ET technique. A hybrid buck converter for the bias modulator, which consists of a linear stage and a switching stage, is optimized for the dynamic load condition according to the envelope level. The measured performances of the CMOS ET PA will be presented and compared to the previously published PAs with efficiency enhancement methods.

II. CMOS POWER AMPLIFIER DESIGN

A schematic of the CMOS PA is depicted in Fig. 2(a). For sufficient gain, the PA consists of two differential stages which have common-source configuration. The PA has off-chip transformers at input and output. Each transformer has a loss of 0.2 dB at the operating frequency of 0.78 GHz. The PA integrated circuit (IC) was implemented using a Magnachip’s standard 0.18-μm CMOS process. Its microphotograph is shown in Fig. 2(b). The size of the chip, including pads, is 0.84 X 0.59 mm². The PA IC was mounted on a printed circuit board (PCB) based on FR-4 for evaluation as shown in Fig. 2(c).

For the measurements of the gain and efficiency, a 0.78 GHz single-tone signal was applied to the PA with various supply voltages from 3.3 to 0.5 V to the drain of the 2nd stage. The 1st stage has a fixed bias of 3.3 V. As shown in Fig. 3(a), a power gain of 27 dB and a power-added efficiency (PAE) of 46 % were achieved at an output power of 27 dBm with a drain bias of 3.3 V. As decreasing the bias voltage from 3.3 to 0.5 V, peak power levels drop but significant PAE improvement was observed at the back-off region. The gain is still higher.
than 20 dB at a bias voltage of 0.5 V.

To measure the third-order inter-modulation distortion (IMD3), a two-tone signal with a center frequency of 0.78 GHz and a tone-spacing of 5 MHz was excited. The measured IMD3 performances with various bias voltages to the drain of the 2nd stage are shown in Fig. 3(b). According to the bias voltages, the output power, satisfying an IMD3 of –30 dBc, drops as well. From these measurement results, we can assign variable bias voltages with respect to the input envelope signal for maximum efficiency improvement while not generating excessive nonlinearity.

### III. Bias Modulator Design

The bias modulator which is based on a hybrid buck converter consists of a wideband linear stage using a class-AB buffer and a highly efficient switching stage, as shown in Fig. 4. The variable output voltage of the bias modulator is supplied to the drain of the PA’s 2nd stage. Hence, the load condition of the bias modulator dynamically changes according to the envelope signal. To properly evaluate the bias modulator, applying the PA as the load is the most accurate way. However, that needs considerable computation time on simulation or is prone to cause convergence error [15].

To save simulation time, we calculated a mean or expected value of the load resistance of the bias modulator using a probability density function (PDF) of envelope signal. A dynamic load resistance for the bias modulator can be extracted from the designed PA using the bias voltage and current to the PA, as shown in Fig. 5. The probability density function (PDF) of the envelope signal for the 16-QAM LTE up-link with a signal bandwidth of 5 MHz is also shown. As shown, the resistance changes from 30 to 10 Ω depending on the envelope voltage. And it looks relatively constant for the envelope signal of more than 1.0 V. The expected load resistance is calculated as follows.
where $p(x)$ is a PDF of $x$. $R_{\text{dyn}}$ is a dynamic load resistance extracted from the PA. As a result, the calculated $R_{\text{exp}}$ of 11.8 $\Omega$ is obtained and used in design of the bias modulator.

Since most of the current from the bias modulator to the PA is supplied from the switching stage, the efficiency of the switching stage is very important for the overall efficiency of the bias modulator. Efficiency of the switching stage is expressed as follows [21].

$$
\eta_{\text{sw}} = \frac{P_{\text{out}}}{(P_{\text{out}} + P_{\text{loss,FET}} + P_{\text{loss,ind}})},
$$

where $P_{\text{out}}$ is an output power of the switching stage, $P_{\text{loss,FET}}$ is a loss of the switch, and $P_{\text{loss,ind}}$ is a loss of the inductor. They are given by

$$
P_{\text{out}} = I_{\text{sw}}^2 \cdot R_{\text{load}},
$$

$$
P_{\text{loss,FET}} = P_{\text{cond}} + P_{\text{sw}} = I_{\text{source}}^2 \cdot r_{\text{on,p}} + I_{\text{sink}}^2 \cdot r_{\text{on,n}} + f_{\text{sw}} \cdot C_{\text{tot}} \cdot V_{\text{DD}}^2,
$$

$$
P_{\text{loss,ind}} = I_{\text{sw}}^2 \cdot R_{\text{DCR}},
$$

where $I_{\text{sw}}$ is an output current of the switch and $R_{\text{load}}$ is a load resistance of the bias modulator. $P_{\text{cond}}$ is a conduction loss and $P_{\text{sw}}$ is a switching loss. $I_{\text{source}}$ and $I_{\text{sink}}$ are the sourcing and sinking current of the switch, respectively. $r_{\text{on,p}}$ and $r_{\text{on,n}}$ are on-resistances of the PMOS and NMOS of the switch. $f_{\text{sw}}$ is a switching frequency and $C_{\text{tot}}$ is a total input capacitance of the switch. $V_{\text{DD}}$ is a supply voltage and $R_{\text{DCR}}$ is a DC-resistance of the inductor.

Both the on-resistances and the total input capacitance of the switch increase the switching loss. The switch size needs to be optimized because the on-resistances and the total input capacitance are inversely and directly proportional to the switch size, respectively. For a load resistance of 12 $\Omega$ and a switching frequency of 2 MHz, the optimized switch size for efficiency is 20 mm X 0.3 $\mu$m and 10 mm X 0.35 $\mu$m for the PMOS and NMOS FETs, respectively.

From [14] and [21], the switching frequency of the hybrid bias modulator is given by

$$
f_{\text{sw}} = \frac{R_{\text{sw}} \cdot V_{\text{sw}} (V_{\text{DD}} - V_{\text{out}})}{2V_{\text{DD}} \cdot N \cdot L \cdot V_{\text{bias}}},
$$

where $R_{\text{sw}}, V_{\text{DD}}, N, L$, and $V_{\text{bias}}$ are a sense resistor, a supply voltage, a current mirroring ratio, an inductance, and a hysteresis of the comparator, respectively. Inductance directly affects the switching frequency and other parameters, such as the current loop bandwidth, ripple voltage, and slew-rate of the switching stage. Therefore, the inductance must be carefully optimized for overall efficiency of the bias modulator [13, 14, 17]. To find an optimum value of the inductor, a number of simulations have been carried out with various inductors at the load of the switching stage. The resultant optimum value of the inductance for the best efficiency and acceptable level of ripple current is 5.8 $\mu$H.

The bias modulator was designed and fabricated using a Magnachip’s 0.18-$\mu$m CMOS process. The fabricated IC is shown in Fig. 6(a). The chip size is 1.55 X 0.7 mm2 including pads. The chip was mounted on FR-4 PCB, as shown in Fig. 6(b), and tested with a supply voltage of 3.3 V for the 16-QAM up-link LTE signal with a signal bandwidth of 5 MHz.

Fig. 7(a) shows the measured waveforms of the envelope output voltage and the switch output voltage with a load resistance of 12 $\Omega$ and an inductance of 5.8 $\mu$H for the 16- QAM LTE up-link signal with a signal bandwidth of 5 MHz. The envelope output voltage was shaped to have a range of from 0.5 to 3.2 V so that the
The average output power of the bias modulator is 25.8 dBm. Switching frequency is observed to be about 2.1 MHz from the measured waveforms.

Fig. 7(b) shows the measured efficiency according to the inductances for an output power of 25.8 dBm. As the inductance decreases, the ripple current gets larger but loss of the inductor becomes smaller. The linear amplifier consumes more power to compensate for the ripple current. As the inductance increases, a loss of the inductor becomes larger. An inductance of 5.8 µH was chosen for the best tradeoff.

Fig. 7(c) shows the measured efficiency versus various load resistances. At a load resistance of 12 Ω, an efficiency of 69% was obtained. Fig. 7(d) shows the measured efficiency according to the output power for a load resistance of 12 Ω. The measured performances of the implemented bias modulator are summarized in Table 1.

Fig. 7. The measured performances of the bias modulator for the 16-QAM LTE up-link signal (a) waveforms, (b) efficiency according to the inductances for an $R_{\text{load}}$ of 12 Ω, (c) efficiency according to the load resistances for an inductance of 5.8 µH, (d) efficiency according to the output power level for an inductance of 5.8 µH and an $R_{\text{load}}$ of 12 Ω.

<table>
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<tr>
<th>Table 1. Performance summary of the bias modulator</th>
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<td>Parameters</td>
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<td>Supply voltage</td>
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<td>Output voltage range</td>
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<td>Unit-gain bandwidth</td>
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<td>Output current</td>
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<td>Efficiency ($R_{\text{out}}$=12 Ω, $V_{\text{dc}}$=3.0 V)</td>
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<td>Efficiency ($R_{\text{out}}$=12 Ω, LTE 16-QAM 5 MHz, $V_{\text{rms}}$=1.9 V)</td>
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### IV. ET PA CONFIGURATION AND MEASUREMENTS

The test bench for the CMOS ET PA is shown in Fig. 8. A baseband signal and an envelope signal for the 16-QAM LTE up-link are generated using Agilent’s Advanced Design System (ADS) and are downloaded...
into the two signal generators. The envelope signal is oversampled using a sampling clock of 92.16 MHz using MATLAB for more precise delay adjustment between the RF path and envelope path.

The voltage waveforms of the envelope signal at the input and output of the bias modulator are monitored using an oscilloscope. The channel power, adjacent channel leakage power ratio (ACLR), and error vector magnitude (EVM) are measured using Agilent’s Vector Signal Analyzer of VAS89600. The 16-QAM LTE up-link signal with a PAPR of 7.3 dB, a signal bandwidth of 5 MHz, and a center frequency of 0.78 GHz was used for the measurements. A single supply voltage of 3.3 V was used for both the bias modulator IC and PA IC.

When the original envelope signal is directly applied to the drain terminal of the PA, the PA generates substantial amplitude modulation to amplitude modulation (AM-AM) and amplitude modulation to phase modulation (AM-PM) distortions. Various envelope shaping methods have been proposed to prevent...
this linearity issue [26]. The shaping functions for various average output power levels, utilized for the ET PA, are shown in Fig. 9. Due to the low knee voltage of the MOSFET, an offset voltage of as low as 0.4 V was used for the shaping functions. The selected shaping functions can effectively improve the efficiency at even back-off power region while the ET PA complies with the E-UTRA’s ACLR specifications. Fig. 10(a) shows the measured gains and PAEs of the ET PA and PA alone. For an average output power of 24 dBm, the PAE of the ET PA is 41.7 % which is 5.3 % higher than that of the PA alone. The PAEs of the ET PA are improved through a wide power range and a maximum improvement of 10.3 % is observed at an output power of 17 dBm. The gain of the PA decreases from 27 dB to 24.7 dB due to the ET operation.

Fig. 10(b) shows the measured E-UTRA ACLR and EVM performances for the ET PA. At an output power of 24 dBm, an ACLR of -30 dBc and an EVM of 4.5 % were achieved for both the ET PA and the PA alone. The measured PSDs are presented in Fig. 10(c) for an average output power of 24 dBm. The performances of the ET PA compared to the PA alone are summarized in Table 2.

The measured performances of the ET PA are compared to the previously published PAs with ET techniques in Table 3. Even though the proposed ET PA circuits were designed only using a standard CMOS process, the performances are comparable to those of the ET PAs whose PAs were designed using compound semiconductor processes.

![Fig. 9. Envelope shaping functions.](image)

![Fig. 10. Measured performances of the ET PA versus the PA alone: (a) PAE and gain, (b) ACLR and EVM, (c) PSDs.](image)

![Table 2. Performance summary for the ET PA and the PA alone using the 16-QAM LTE up-link signal](table)
V. CONCLUSIONS

In this paper, the ET PA ICs based on a standard 0.18-μm CMOS process is presented. The PA is designed and optimized to have a two-stage differential commonsource structure for high gain, high power, high efficiency, and better ET operation. For the bias modulator, the switching amplifier is optimized under consideration of a dynamic load condition.

The implemented CMOS ET PA circuits are evaluated using a 16-QAM LTE up-link signal with a signal bandwidth of 5 MHz and a PAPR of 7.3 dB at a center frequency of 0.78 GHz. A measured PAE of 41.7 % at an average output power of 24 dBm was achieved using the ET PA, while the PA alone exhibited 5.3 % lower PAE at the same condition. Applying the optimized envelope shaping function, almost no linearity degradation from the performance of the PA alone was observed for the ET PA at high output power region. The full CMOS based ET PA in this work exhibited comparable output performances to the previously published ET PAs even using the PAs based on compound semiconductor processes.

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