A Highly Power-Efficient Single-Inductor Multiple-Outputs (SIMO) DC-DC Converter with Gate Charge Sharing Method

Ki-Soo Nam, Whan-Seok Seo, Hyun-A Ahn, Young-Ho Jung, Seong-Kwan Hong, and Oh-Kyong Kwon

Abstract—This paper proposes a highly power-efficient single-inductor multiple-outputs (SIMO) DC-DC converter with a gate charge sharing method in which gate charges of output switches are shared to improve the power efficiency and to reduce the switching power loss. The proposed converter was fabricated by using a 0.18 µm CMOS process technology with high voltage devices of 5 V. The input voltage range of the converter is from 2.8 V to 4.2 V, which is based on a single cell lithium-ion battery, and the output voltages are 1.0 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V. Using the proposed gate charge sharing method, the maximum power efficiency is measured to be 87.2% at the total output current of 450 mA. The measured power efficiency improved by 2.1% compared with that of the SIMO DC-DC converter without the proposed gate charge sharing method.

Index Terms—DC-DC converter, single inductor multiple outputs (SIMO), power efficiency, charge sharing, switching power loss

I. INTRODUCTION

Recently, mobile devices such as smart phone, tablet PC, and other handheld applications have gained popularity because of their portability, usability, accessibility, and excellent performances [1-3]. To make these mobile devices more efficient, many researches on various fields, such as display, application processor, sensors, and power management ICs, have been performed. Among these researches, more efforts are focused on improving the performance of supply voltage management ICs which is the most influential to all components in mobile devices.

In mobile devices, the supply voltages are mainly generated from their batteries by using low-dropout (LDO) regulator, charge pump, or inductive switching converter. The LDO regulator has high accuracy, but its power efficiency heavily depends on input and output conditions [1-3]. The charge pump requires no external components, but has low accuracy, moderate power efficiency, and poor current driving capability [3]. The inductive switching converter has high power efficiency and large current driving capability, but requires external inductor and capacitor. However, it is not practical to use multiple external inductors in generating multiple supply voltages which are required for mobile devices [3-12].

In [4-12], the single-inductor multiple-outputs (SIMO) DC-DC converter was introduced to generate the required supply voltages without increasing the number of external inductors. This SIMO DC-DC converter uses only one inductor to generate multiple outputs. In SIMO DC-DC converter, however, power efficiency and regulation characteristics are worse than those of typical inductive switching converter with single-output. Although the deterioration of regulation characteristic
has been partially overcome by various researches and efforts [10-12], it is still difficult to improve the power efficiency of the converter because of switching and conduction power losses at multiple output switches in the SIMO DC-DC. In this paper, a SIMO DC-DC converter with gate charge sharing method, in which gate charges of output switches are shared, is proposed to reduce the switching power loss and improve the power efficiency for mobile applications.

II. THE PROPOSED SIMO CONVERTER

1. Structure and operating principle

Fig. 1 shows the block diagram of the proposed SIMO DC-DC converter. In the proposed converter, the current programed mode control converter topology is adopted and only one inductor is used to generate five outputs (V_{o.1}, V_{o.2}, V_{o.3}, V_{o.4}, and V_{o.5}). The proposed converter consists of two main control switches (M_p and M_n), five output switches (M_{o.1}, M_{o.2}, M_{o.3}, M_{o.4}, and M_{o.5}), five output capacitors (C_{o.1}, C_{o.2}, C_{o.3}, C_{o.4}, and C_{o.5}), an inductor, a freewheeling switch (M_{fw}), a main control block, and six gate charge control blocks. The main control block consists of a voltage feedback block, a current feedback block, a mode control block, a pulse width modulation (PWM) controller, a gate driver, an oscillator (Osc.), and a band-gap reference generator (BGR). Five gate signals of output switches are generated by gate charge control blocks. All output switches are connected together at V_x and gate charge control blocks are connected each other at V_{sh} to share the gate charges using the proposed gate charge sharing method. To prevent the body diode of PMOS switches from being turned on, a body node of each PMOS switch is biased to the higher of the source and drain voltages of each PMOS switch. The range of input voltage (V_{in}) is from 2.8 V to 4.2 V, which is the voltage range of a single cell lithium-ion battery, and five output voltages are 1.0 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V. The proposed converter is designed to supply the total current of 1 A, and each output switch is designed to have the driving capability of 200 mA.

The switching operation of M_p and M_n energizes inductor, and the energy of inductor is supplied to each output sequentially. When the gate charge control block receives the trigger signal (V_{1,0-1}) from previous gate charge control block, the gate charge control block turns on the output switch. The n is integer from 1 to 5. Then, the inductor provides energy to the output and the output voltage is increased to the target voltage. When the gate charge control block senses that the output voltage reaches target voltage, the gate charge control block turns off the output switch and sends a trigger signal (V_{1,n}) to the next gate charge control block. The difference between the energy induced in the inductor and that required at every output is accumulated as voltage error at the last output, and the main control block determines on-duty of main control switches to reduce the voltage error of the last output.

To generate the last output voltage securely when the input voltage is lower than the highest output voltage (V_{o.5}), the proposed converter is adaptively operated in buck and buck-boost modes according to the input voltage level. When V_{in} is higher than V_{o.5}, the proposed converter is operated in buck mode. In this case, the proposed converter operates like the conventional SIMO buck mode converter. When V_{in} is lower than V_{o.5}, the proposed converter operates in buck-boost mode. In this case, M_p is turned on and M_n is turned off to drive the last output voltage when V_{1,4} becomes high. Consequently, the input voltage is directly supplied to the last output, and the last output voltage is determined by adding the input voltage to the induced voltage of the inductor.
Fig. 2 shows the block diagram of mode control block and PWM controller. In the mode control block, \( V_{in} \) is compared to \( V_{o.5} \), and the operation mode signal (\( V_{mode} \)) is determined by comparator. When \( V_{in} \) is higher than \( V_{o.5} \), \( V_{mode} \) becomes low and thereby the buck mode is selected. When \( V_{in} \) is lower than \( V_{o.5} \), \( V_{mode} \) becomes high and thereby the buck-boost mode is selected. The PWM controller generates the trigger signal (\( V_{t.0} \)) of first gate charge sharing block for gate charge sharing operation and on-duty signal (\( V_{on-duty} \)) of gate driver according to \( V_{mode} \), and voltage and current feedback data (\( V_{vfb} \) and \( V_{cfb} \)). The \( V_{on-duty} \) becomes low by positive-type one-shot and \( V_{t.4} \), in buck and buck-boost modes, respectively. The \( V_{on-duty} \) becomes high when \( V_{cfb} \) is higher than \( V_{vfb} \).

Fig. 3 shows the simulation results of gate signals of main and output switches in buck and buck-boost modes. \( V_{Mp} \) and \( V_{Mn} \) are switched to energize the inductor, and the on-duty of \( V_{Mp} \) and \( V_{Mn} \) is determined by voltage and current feedback blocks. Each output switch turns on and off sequentially to supply the energy in inductor to each output. Operations of \( V_{Mp} \) and \( V_{Mn} \) in Fig. 3(a) are similar to those in conventional buck converter. On the other hand, operations of \( V_{Mp} \) and \( V_{Mn} \) in Fig. 3(b) are different from those in conventional buck converter. To perform the boost operation at the last output, \( V_{Mp} \) and \( V_{Mn} \) become low, and thereby the proposed converter supplies sum of the input voltage and the induced voltage of the inductor to the last output voltage.

2. Gate charge control block

The block diagram of gate charge control and body bias control blocks in \( n^{th} \) output is shown in Fig. 4. The \( n \) is integer from 1 to 5. The gate charge control block consists of a comparator, a sharing switch (\( S_{share,n} \)), a

Fig. 4. Block diagram of gate charge control and body bias control blocks.
driving switch (S_{drive,n}), a gate driver, an edge triggered D flip flop, a delay cell, a positive-type one-shot, a negative-type one-shot, a NOR gate, an inverter, and a current sensor. The comparator senses whether each output voltage reaches target voltage or not. The positive-type and negative type one-shot blocks determine the period of a sharing phase, which is on-duty of the sharing switch. The current sensor senses current through output switch (M_{s,n}) and provides current feedback data (I_{ref}) to the main control block. In the body bias control block, the source voltage of each PMOS is compared to its drain voltage by a comparator and a body node of each PMOS switch is biased to the higher of the source and drain voltages of each PMOS switch to prevent the body diode of PMOS switches from being turned on.

When the trigger signal (V_{in-1}) of the previous gate charge control block is high, the output of edge triggered D flip flop becomes high and the S_{share,n} is turned on by negative-type one-shot and NOR gate during the sharing phase. In the sharing phase, the S_{share,n} connects the gate node (V_{s,n}) of output switch to gate node (V_{s,n+1}) of previous output switch (M_{s,n-1}), and thereby gate charges of two output switches (M_{s,n-1} and M_{s,n}) are shared. By the gate charge sharing method, the gate voltages (V_{s,n-1} and V_{s,n}) of two output switches become the same as half of V_{DD} if gate capacitances of two output switches are the same. During the sharing phase, the interference between two output voltages is occurred, but the ripple of output voltage by the gate charge sharing operation is negligible because the period of sharing phase is much smaller than RC time constant, which is determined by the on-resistance of output switch and the capacitance of output capacitor (C_{on}). In the proposed converter, the maximum ripple of output voltage is designed to be less than 80 mV. The ripples of output voltage by the gate charge sharing operation and by the regulating operation of converter do not appear simultaneously. Therefore, the ripple of output voltage by the gate charge sharing operation is designed to be smaller than 80 mV. After the sharing phase, S_{share,n} is turned off and S_{drive,n} is turned on. In driving phase, the S_{drive,n} connects the output of the gate driver to the V_{s,n}. The gate driver drives the V_{s,n} from half of V_{DD} to V_{SS} and the M_{s,n} is fully turn on because the output of edge triggered D flip flop is still high. Then, the M_{s,n} supplies the induced energy of inductor to the output.

When the V_{th,n} becomes higher than V_{ref}, the output of edge triggered D flip flop becomes low, and the S_{share,n} is turned on by positive-type one-shot and NOR gate during the sharing phase. Moreover, the trigger signal (V_{in}) is high and thereby the sharing switch (S_{share,n+1}) of the next gate charge control block is turned on. Then, gate charges of two output switches (M_{s,n} and M_{s,n+1}) are shared and gate voltages (V_{s,n} and V_{s,n+1}) of two output switches become the same as half of V_{DD}. After the sharing phase, S_{drive,n} is turned on and the gate driver drives the V_{s,n} from half of V_{DD} to V_{DD}. The switching power loss of output switch is given by

\[ P_{\text{loss, switching}} = V_{DD} \times \frac{C_{\text{gate}} \times \Delta V_{\text{swing}}}{\Delta t} = V_{DD} \times \frac{C_{\text{gate}} \times \frac{1}{2} V_{DD} \times f}{\Delta t} = \frac{1}{2} C_{\text{gate}} \times V_{DD}^2 \times f \]

where \( P_{\text{loss, switching}} \) is the switching power loss, \( V_{DD} \) is the supply voltage, \( C_{\text{gate}} \) is the gate capacitance of output switch, \( \Delta V_{\text{swing}} \) is the driven voltage by the gate driver, \( \Delta t \) is the switching period, and \( f \) is the switching frequency of converter. It is calculated that the switching power loss is halved by the proposed gate charge sharing method.

Fig. 5 shows the simulation results of gate charge control block for three outputs. The \( k \) is integer from 1 to 3. In the sharing phase, two sharing switches are turned
on and the gate charges of two output switches are shared. During the sharing phase for $k^{th}$ and $(k+1)^{th}$ output switches, the gate voltage ($V_{s,k}$) of $k^{th}$ output switch is increased and the gate voltage ($V_{s,k+1}$) of $(k+1)^{th}$ output switch is decreased. In the driving phase, sharing switches are turned off and $k^{th}$ and $(k+1)^{th}$ output switches are fully turned on and off by gate drivers, respectively.

III. MEASUREMENT RESULTS

The proposed converter is fabricated by using a 0.18-μm CMOS process technology with high voltage devices with the operation voltage of 5 V. Fig. 6 shows the layout of the proposed converter whose chip area is $2,000 \times 2,000 \mu m^2$. The gate area of one output switch is $20,000 \mu m^2$ and the area of one gate charge control block is $200 \times 125 \mu m^2$. The printed circuit board (PCB) to verify the proposed converter is shown in Fig. 7. An inductor of 10 μH was selected in regard to the output current and ripple characteristics of output voltages.

Fig. 8 shows the test results of $S_{\text{share},1}$ and $V_{s,1}$ for the proposed gate charge sharing method. When the gate voltage of output switch is varied, the sharing switch is verified to be turned on. The period of sharing phase is designed to be 20 nsec which is enough time for gate charge sharing operation considering the gate capacitance.

Figs. 9(a) and (b) show test results of output voltages when input voltages are 4.2 V and 2.8 V, respectively. In these cases, the last output voltage is generated securely by buck and buck-boost mode operation. Measurement results show that the ripples of output voltage by the gate charge sharing operation and the regulating operation of the converter are 30 mV and 70 mV, respectively. Because the ripple of output voltage by the gate charge sharing operation is smaller than that by the regulating operation of the converter, an additional fluctuation of output voltage by the interference between two output voltages is negligible. Fig. 10 shows power efficiency of the SIMO DC-DC converter with and without the proposed gate charge sharing method. Using the proposed gate charge sharing method, the maximum power efficiency is measured to be 87.2% at the total output current of 450 mA, and the power efficiency improved by 2.1% compared with that of the SIMO DC-DC converter without the proposed gate charge sharing.
method. In Table 1, the performance of the proposed SIMO converter is summarized and compared with the previous works, showing higher maximum power efficiency.

### IV. CONCLUSIONS

A SIMO DC-DC converter with gate charge sharing method is proposed to improve the power efficiency. Gate charges of output switches are shared to improve the power efficiency and to reduce the switching power loss. In order to generate the last output voltage securely when input voltage is lower than the last output voltage, the proposed converter operates adaptively in buck and buck-boost modes according to the input voltage with wide operating voltage range. Using the proposed gate charge sharing method, the maximum power efficiency is measured to be 87.2% at the total output current of 450 mA, and the power efficiency improved by 2.1% compared with that of the SIMO DC-DC converter without the proposed gate charge sharing method. Therefore, the proposed SIMO DC-DC converter is very suitable for mobile applications.

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**Table 1. Performance summary and comparison**

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<td>0.35 μm</td>
<td>65 nm</td>
<td>0.18 μm</td>
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<td>Input voltage (V)</td>
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<td>2.7 ~ 5.0</td>
<td>3.4 ~ 4.3</td>
<td>2.8 ~ 4.2</td>
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<td>Output voltages (V)</td>
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<td>1.0, 1.2, 1.8, 2.5, and 3.3</td>
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<td>Max. power efficiency (%)</td>
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<td>Frequency (MHz)</td>
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<td>1.2</td>
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<td>Load regulation (mV/mA)</td>
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<td>Cross-regulation (mV/mA)</td>
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<td>0.067</td>
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**Fig. 9.** Test results of output voltages ($V_{o.1}$, $V_{o.3}$, and $V_{o.5}$) (a) Buck mode operation at input voltage of 4.2 V, (b) Buck-boost mode operation at input voltage of 2.8 V.

**Fig. 10.** Power efficiency of the SIMO DC-DC converter with and without the proposed gate charge sharing method.
**REFERENCES**


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