Dynamic Slew-Rate Control for High Uniformity and Low Power in LCD Driver ICs

Sung-Pil Choi¹,², Mira Lee², Jahoon Jin¹, Kee-Won Kwon¹, and Jung-Hoon Chun¹

Abstract—A slew-rate control method of LCD driver ICs is introduced to increase uniformity between adjacent driver ICs and reduce power consumption. The slew rate of every voltage follower is calibrated by a feedback algorithm during the non-displaying period. Under normal operation mode, the slew rate is dynamically controlled for improving power efficiency. Experimental results show that the power consumption is reduced by 16% with a white pattern and by 10% with a black pattern, and display defects are successfully eliminated.

Index Terms—DDI, LCD driver IC, slew rate, high uniformity, charge recycling

I. INTRODUCTION

Preferences for high-definition displays require faster operation of display solutions such as timing controllers and display driver ICs (DDIs). There are several requirements for the DDIs of high-definition displays. First, a uniform analog characteristic in the time domain should be achieved. For example, the output drivers that supply the current for the storage capacitors in the LCD cells should have an identical slew rate, because the transparency of an LCD cell is determined by the voltage levels across the storage capacitors. Otherwise, a discrepancy in the slew rate of a DDI causes a difference in the voltage levels between adjacent LCD cells and then introduces vertical color discordance, as depicted in Fig. 1(a). An RC load, which is an equivalent model of an LCD panel, causes delays corresponding to the distances from the outputs of the DDI to each LCD cell. If the delay causes a difference in the voltage levels between the top area and the bottom area when the corresponding gate line is selected, the brightness of the LCD varies gradually, as shown in Fig. 1(b). In order to alleviate these display defects, the slew rate of the DDI is usually designed to be extremely fast [1, 2]. However, a faster slew rate is accompanied by an increase in the power consumption as well as higher radiation of EMI.

There have been several efforts to reduce the power consumption of the DDIs [3, 4]. Reference [3] decreased the dynamic power consumption by reducing the frame frequency. However, this proposal could not decrease the power consumption when displaying a moving picture because a low frame rate can cause a flicker phenomenon. Reference [3] also requires additional on-chip memory with a capacity equal to “vertical resolution × horizontal resolution × color depth,” so this proposal is not easily applied to applications with resolution over FHD (1920 × 1080). Reference [4] reported an algorithm to overcome the variation in the RC delay due to the LCD load. However, reference [4] controlled CMOS switches connected to the output stage in the DDI, that sustains a static bias current. This method has the possibility of unstable operation because the varying transconductance (gm) of the output stage affects the phase margin of the loop with the voltage follower. The goal of this work is to decrease the power consumption of DDIs, with the enhancement of the display quality. The proposed circuit and its operation mechanism will be described in Section 2. Simulation results and measurement results will be
The proposed DDI consists of a receiver, a deserializer, shift registers, data latches, a digital-to-analog converter, voltage followers, and slew-rate control (SR_CONTROL) block, as in Fig. 2. The receiver (Rx) restores the differential-mode signals from a panel processor or an application processor, and then the deserializer rearranges the data into binary order. The shift registers and latches store the corresponding binary-order data. These data are converted to an analog level by the digital-to-analog converter and transferred to a display panel, through the voltage followers. In DDIs, the voltage followers are critical in determining display qualities, overall power consumption, and thermal characteristics.

1. Circuits for Improving Inter-chip Uniformity

Among the characteristics of the voltage follower, the slew rate is sensitive to process variations. In order to overcome the variation in the slew rate, we propose a calibration method for voltage followers by using a feedback loop, as in Fig. 2. The feedback loop starts with the rising edge of “cal_mode”. During the calibration mode, \( VBIAS\_TOP/CEN/BOT \) are sequentially connected to \( VBIAS \) through the mux (VBIAS_SEL). However, at first we assume that \( VBIAS\_TOP \) is routed to \( VBIAS \) for the convenience of comprehension. The roles of \( VBIAS\_CEN/BOT \) and their relevant signals, \( TARG\_CEN/BOT \) will soon be explained in the next section. \( VBIAS \) determines the bias current \( I_{BIA} \) from the BIAS block. \( I_{BIA} \) is supplied to the voltage follower and the replica of the voltage follower in SLEW_GEN. SLEW_GEN generates the time flags for the starting and ending of a slewing behavior of the voltage follower. A time-to-digital converter (TDC) in CTRL_BIAS converts the timing difference between two time flags to a digital code. This TDC output is compared with \( TARG\_TOP \) which is the pre-determined target value for the slewing period. Reflecting the comparison result, \( VBIAS\_TOP \) is adjusted so that the TDC output becomes equal to \( TARG\_TOP \). When the calibration is completed, a flag signal (cal_done) is asserted and the feedback loop is terminated.

Fig. 3(a) shows a structural diagram of SLEW_GEN. The vertical synchronization signal (VSYNC), indicating the start of every frame is a reset signal for SLEW_GEN. SLEW_GEN generates the “SLEW_START” and “SLEW_END” signals. The rising edge of SLEW_START, which is interlocked with the rising edge of the horizontal synchronization signal (HSYNC),
indicates the start of line scanning. At the rising edge of SLEW_START, the input of a replica of the voltage follower in a DDI is switched from the low \( \gamma \) voltage (1 V), to the high \( \gamma \) voltage (5 V). Then, the output of the voltage follower traces an input voltage, with a slew rate determined by the bias current, \( I_{BIAS} \). A comparator, COMP creates the falling edge of SLEW_ENDB, when the output of a voltage follower passes through the reference gamma voltage level (4 V). During the period from the rising edge of SLEW_START to the falling edge of SLEW_ENDB, CTRL_BIAS counts the number of internal clocks, and then compares the counted value, \( COUNT \), with a target value, \( TARG_TOP \). If \( COUNT \) is smaller than \( TARG_TOP \), the binary value of \( VBIAS_TOP \) is increased every HSYNC cycle. Because the binary weighted resistors in BIAS are connected in parallel as depicted in Fig. 3(b), \( I_{BIAS} \) and the slew rate of the voltage follower linearly increase as \( VBIAS \) which is the same as \( VBIAS_TOP \) increases. When \( COUNT \) becomes larger than the target value, CTRL_BIAS changes the direction of \( VBIAS_TOP \) to downward. A history register (DIR_HIST) is also embedded for stable operation. Whenever the values of \( COUNT \) and \( TARG_TOP \) are the same, the value of DIR_HIST is increased by one. Finally, when the value of DIR_HIST reaches seven as in Fig. 4, a flag (BIAS_LOCK) is switched to one, and the feedback loop of CTRL_BIAS block is terminated. Then, the value of \( VBIAS_TOP \) is sustained. The overall operations are summarized as a flow-chart in Fig. 5.

Fig. 3. (a) Structural diagram for SLEW_GEN, (b) Bias current generating circuit in BIAS block.

Fig. 4. Timing diagram of CTRL_BIAS block for the slew-rate calculation.

Fig. 5. Flow-chart of the operation of SR_CONTROL block.
2. Circuits for Reducing the Power Consumption

Fig. 6 shows a five-stage RC-load model of an FHD resolution (1920 × 1080) LCD panel. Because full color for an LCD panel is composed of the three elementary colors (Red/Green/Blue), FHD resolution can be supported by 5760 (= 1920 × 3) voltage followers. In Fig. 6, the driver output nodes are represented as Y1-Y5760, and VCOM is a virtual ground for the display panel. The RC delay of the transparent metal lines from a voltage follower to each LCD cell can be analyzed by the Elmore load model. \( T_{Ed,M,N} \) is the delay from a driver output node to the top area of the equivalent RC-load model with total \( N \) stages [5].

\[
T_{Ed,M,N} = \frac{RC}{2} \left\{ N^2 - (N-M) \right\}
\]

With \( N = 5 \), the calculated delay from the driver output to the top area \( (M = 1) \) of the LCD panel is ‘4.5 × RC’; whereas, the delay to the bottom node \( (M = N = 5) \) is ‘12.5 × RC’.

A conventional DDI has a fixed driving strength, irrespective of the positions inside an LCD panel; thus, the slew-rate of the driver is determined by the longest RC delay at the bottom area. Therefore, the rising time is considerably shorter than necessary when the voltage follower of the DDI drives another area of the LCD panel.

To decrease this unnecessary power consumption due to an extra fast slew rate for driving center and top area of LCD panel, we dynamically adjust the driver strength as the target of the driving signal alters. We divide an entire LCD panel into three areas (top/center/bottom) and allocate each section a slew-rate target value. That is, \( TARG_{TOP} \) in Fig. 2 indicates the target value of the slewing period when the DDI drives the top area of the display panel. \( TARG_{CEN} \) and \( TARG_{BOT} \) are target values when DDIs drive the center and bottom areas of the panel, respectively. In the calibration mode, \( VBIAS_{TOP/CEN/BOT} \) are sequentially connected to \( VBIAS \), and calibrated according to \( TARG_{TOP/CEN/BOT} \) values. Once \( VBIAS_{TOP/CEN/BOT} \) are calibrated, they are used in dynamic control of the slew rate, under normal operating conditions.

Dynamic control of the slew rate is performed by counting the HSYNC signal. Fig. 7 shows the detailed schematic of \( VBIAS_{SEL} \) which was introduced in Fig. 2. For the first 360 periods of HSYNC, \( VBIAS_{TOP} \) is connected to \( VBIAS \), and the slew rate is set according to \( TARG_{TOP} \). When the 361st pulse arrives at \( VBIAS_{SEL} \), \( VBIAS_{CEN} \) is routed to \( VBIAS \), and the slew rate is set to \( TARG_{CEN} \). After the next 360 periods, \( VBIAS \) is once again changed to \( VBIAS_{BOT} \), and the slew-rate is increased to \( TARG_{BOT} \), to compensate for the additional delay through the metal lines in the panel. To prevent the injection of the switching noise, alternations from one target value to the next target value occur when the output of a voltage follower is in the Hi-Z state and in the process of charge-recycling. The role and the details of the charge-recycling are explained below.

Fig. 8(a) shows how multiple voltage followers are connected to an LCD panel. To avoid solidification of the liquid crystal, the output of each driver should
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Alternate its polarity every time, which results in considerable dynamic power consumption. Because $Y_{2k}$ and $Y_{2k+1}$ have opposite polarity, charge recycling can be used to reduce power consumption. The timing diagrams of the adjacent driver outputs ($Y_{2k}$ and $Y_{2k+1}$) and other related signals are depicted in Fig. 8(b). After $HSYNC$ rises, the “AMP$OUT\_EN$” signal drops and the output of a voltage follower is cut off from the LCD panel. Then, the “CR$\_EN$” signal is set high, and the charge recycling process begins. That is, the internal charges are compensated for by two voltage follower outputs with opposite polarities while CR$\_EN$ is kept high. Right after CR$\_EN$ goes low, and the charge recycling is over, AMP$OUT\_EN$ is set to high, and the drivers are once again connected to the panel.

III. SIMULATION RESULTS

Fig. 9 shows the simulated results for a voltage follower in a DDI. As shown in Fig. 9(a), the output obtains a corresponding RC delay, when passing through an LCD load. This is a typical characteristic of a conventional DDI, with a fixed driving strength. The rising time, when driving the top area of an LCD panel, is only 0.69 us. However, the LCD panel load increases the rising time of a voltage follower to 1.87 us at the bottom area. The ratio between these two values reaches 2.71, and is slightly different than the theoretical value of 2.78 ($=12.5/4.5$) from [5]. In the proposed control method, we assign four-bit binary codes as 1011'b for TARG$\_TOP$, 1000'b for TARG$\_CEN$, and 0010'b for TARG$\_BOT$.
TARG_BOT, as in Fig. 2. The output of a voltage follower exhibits a different rising time at the connection point between a DDI and the LCD panel, as shown in Fig. 9(b). However, the rising times show only a negligible difference in Fig. 9(c), when we probe the output at each targeted area. The rising time is 1.78 μs at the top area, 1.77 μs at the center area, and 1.87 μs at the bottom area.

In Fig. 10, the power consumption is simulated according to several display patterns. Because the supply voltage is identical, the averaged current is plotted instead. The conventional DDI sustains a constant current consumption irrespective of the areas of the LCD panel. However, the current consumption of the proposed DDI varies with the areas. While the same current is necessary for driving the bottom area of the LCD panel, the current consumption is decreased for other areas. The difference between the conventional DDI and the proposed DDI is largest at the top area. Because the voltage level close to VCOM represents white color for a TN-mode LCD [6], a white pattern results in the smallest voltage swing and current consumption. In contrast, a black pattern exhibits the largest voltage swing, and consumes the largest current, when changing the polarity, when we focus only on the operation of a voltage follower. The other blocks in the DDI, except for a voltage follower, also consume considerable current when the display data changes as e.g. a sub-dot pattern. So, the overall current consumption for the sub-dot pattern is larger than that for the black pattern. However, it should be noted that the reduction in the current consumption is valid irrespective of the display pattern. The simulation results show a reduction ratio of 10% with the sub-dot pattern, 12 % with the black pattern, and 16% with the white pattern.

IV. FABRICATION AND MEASUREMENT

We fabricated the proposed DDI using a 0.25-μm CMOS process. Fig. 11 shows the full-chip layout of the proposed DDI. The entire DDI with 576 followers occupies 21 mm². We tested the DDIs with a 55” FHD LCD panel of which the total RC load is 10 kΩ, 200 pF. Fig. 12 shows the photographs of the test setup with the LCD panel. 10 DDIs are located on the film between the DDI PCBs and the LCD panel. The power board at the bottom right corner generates various power supply voltages, and the PCB at the bottom left corner includes a timing controller and an I2C interface.

Fig. 13 shows the photographs for the evaluation of the DDIs. An LCD panel with conventional DDIs successfully produces white color at the top-side as shown in Fig. 13(a). However, a dark gray color is present, owing to a slow slew rate at the bottom-side of the LCD panel. Between these two positions, the LCD panel suffers a gradual difference in brightness. In contrast, the proposed method for controlling the rising time effectively eliminates this display defect as shown in Fig. 13(b). The measured results for the rising time are shown in Fig. 14. Here, the rising time of a voltage follower is defined as the period from the start of the charge recycling to the point when the output of the voltage follower reaches 90% of a target voltage level. Because the graph is plotted using a massive data set composed of several thousand DDIs, the standard
deviation of this distribution indicates the uniformity of the slew rate. The rising time has an average value of 2.57 μs, with a standard deviation of 0.08 μs, for the conventional DDI and an average value of 2.70 μs, and a standard deviation of 0.05 μs, for the proposed DDI with 1111’b for TARG_TOP. Even though the average value of the proposed DDI is greater than that of the conventional DDI, the standard deviation of the proposed DDI is smaller than that of the conventional DDI. Thus, the uniformity of the slew rate is successfully enhanced, by using the proposed circuit.

Fig. 15 shows the measured output waveforms of the proposed DDI with the black pattern. Three waveforms show the calibrated slew-rates driving each of the bottom/center/top side of the LCD panel. The slew rate for the top-side of the LCD panel is decreased by 0.6 μs compared with that at driving the bottom side.

Table 1 lists the measured overall current consumption of a DDI with various display patterns. The current consumption is reduced by ~16% for the white pattern, and ~10% for the black and sub-dot patterns.

V. CONCLUSION

We proposed dynamic slew-rate control for high-uniformity and low power consumption for a DDI and provided experimental results. Compared to the conventional DDI, the proposed DDI successfully eliminated display defects and decreased the overall current consumption by 10%~12%.
ACKNOWLEDGMENTS

This research was supported by the MPIS, Korea, under the ITRC support program (NIPA-2014-H0301-14-1008) supervised by the NIPA.

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Sung-Pil Choi is a Ph.D candidate at Sungkyunkwan University, Korea. He received his B.S and M.S. degrees in electrical engineering from Seoul National University, Korea, in 2000 and 2002, respectively. In 2001, he worked for TomatoLSI, Seoul, where he developed several LCD driver ICs for mobile application. He moved to Samsung Electronics in 2004 and worked in the areas of Display Driver IC. He has been developing several Display Driver ICs for large display panel. His current research is UHD & QUHD driving technology and low-power design of a Display Driver IC for tablet display.

Mira Lee received her B.S and M.S. degrees in electrical engineering from Sungkyunkwan University, Korea, in 2011 and 2013, respectively. In 2011, she joined Samsung Electronics, Giheung, Korea. She has been working on CMOS image sensors for mobile device cameras. She is also currently co-working with Sungkyunkwan University, in the area of low-power serial links design.

Jahoon Jin received the B.S degree in Electrical engineering from Sungkyunkwan University, Korea, in 2013. He is currently pursuing the Ph.D. degree at the same university. His research interests include analog and digital circuit design for high-speed serial links.
Kee-Won Kwon received his B.S. degree in metallurgical engineering from Seoul National University, in 1988. He also received his M.S. degree in electrical engineering and the Ph.D. degree in materials science and engineering from Stanford University, Stanford, CA, in 2000 and 2001, respectively. From 1990 to 1995, he was with Samsung Electronics, Giheung, Korea, where he developed tantalum pentoxide dielectric thin films and successfully implemented them into the commercial product of DRAM. In 2000, he worked for Maxim Integrated Products, Sunnyvale, CA where he was involved in two projects of data converting circuit design. He rejoined Samsung Electronics in 2001, and worked in the areas of high performance DRAM designs including Rambus DRAM and XDR DRAM. In 2007, he moved to Sungkyunkwan University, where he is doing research on memory IP design, and low power high speed circuit solutions for analog and mixed-signal devices.

Jung-Hoon Chun is an Associate Professor at Sungkyunkwan University, Korea. He received his B.S. and M.S. degrees in electrical engineering from Seoul National University, Korea, in 1998 and 2000, respectively. In 2006, he received his Ph.D. degree in electrical engineering from Stanford University. From 2000 to 2001, he worked at Samsung Electronics where he developed BiCMOS RF front-end IC for wireless communication. From 2006 to 2008, he was with Rambus Inc. where he worked on high-speed serial interfaces such as FlexIO™, XDR™, and XDR2™. Dr. Chun also consults for several IC design and foundry companies in Korea and Silicon Valley. His current research includes high-speed serial link, on-chip ESD protection and I/O design, new memory devices, etc.