A CMOS Hysteretic DC-DC Buck Converter with a Constant Switching Frequency

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Abstract—This paper describes a CMOS hysteretic DC-DC buck converter with a constant switching frequency for mobile applications. The inherent problems of a large output ripple voltage that the conventional hysteretic DC-DC buck converters has faced have been resolved by using the proposed DC-DC buck converter which employed a ramp generator circuit to be able to increase a switching frequency. The proposed architecture enables the settling response time of charge pump circuit within the converter to become less than 6us suitable for mobile applications. The proposed DC-DC buck converter was implemented by using 0.35 um BCDMOS process and die size was 1.37 mm x 1.37 mm. The measurement results showed that the proposed circuit received the input of 3.7 V and generated output of 1.2 V with the output ripple voltages less than 20 mV under load currents of 100~400 mA at the fixed switching frequency of 2 MHz. The maximum efficiency of the proposed hysteretic buck converter was measured to be around 93%.

Index Terms—Hysteretic buck converter, ramp generator, delay time control circuit, switching frequency, mobile applications

I. INTRODUCTION

It has been found in the literature [1, 2] that the conventional hysteretic buck converter inherently showed faster transient response with various load currents than the conventional buck converters which employed different kind of feedback methods such as PWM voltage and current mode control. The other advantage of the hysteretic buck converters over conventional PWM buck converters are the inherent simple circuit architecture because of no compensation circuit required. However, they suffered from not only EMI problem due to the switching frequency to be continuously changing, but also a large output ripple voltage due to the wide hysteresis window range. The conventional hysteretic buck converters heavily based upon logic circuits generated a relatively large ripple output voltages due to logic switching.

The inherent switching frequency of the conventional hysteretic converter becomes too low not only to employ small power inductor, but also to make output ripple small. The proposed circuit employed a ramp generator, a CCM/DCM selection circuit and a delay time control circuit with a phase locked loop (PLL) architecture to resolve the problems conventional hysteretic converter suffered. The rest of this paper is organized as follows. Section 2 describes the proposed architecture and design of the main block. The simulation and measurement results are presented and discussed to compare the performances of the proposed circuit with those of the conventional circuits in Section 3. Finally, the conclusions are drawn in Section 4.

II. THE PROPOSED ARCHITECTURE

The overall architecture of the proposed circuit in this section is presented in Fig. 1. The on-chip circuit is within the dotted line. The off-chip circuit outside the
dotted line includes an inductor (L), two capacitors (C₀, CFB), a load, and a feedback resistor (RFB). The proposed on-chip circuit consists of the conventional hysteretic buck converter with a ramp generator, a band gap reference circuit, a delay control circuit, 2 to 1 multiplexer, continuous conduction mode (CCM)/discontinuous conduction mode (DCM) selection circuit, a zero current detector, a dead time control circuit with buffer, a n-channel power switch, and a p-channel power switch. The positive input node of the hysteresis comparator is connected to the band gap reference circuit. The negative input node (V_FB) of the hysteresis comparator is connected to both the feedback resistor, RFB and the output of the ramp function generator, so that the output voltage (V_OUT) is added to the ramp signal from the ramp generator.

The resultant output signal (D) from the hysteresis comparator is applied to both the input of the 2:1 multiplexer and the phase frequency detector within the delay time control circuit. The phase frequency detector circuit drives the charge pump circuit, so that it determines the magnitude of the control voltage, V_CTRL of the second order frequency compensation circuit. The delay time, D_DELAYED from the delay control circuit is determined by the control voltage, V_CTRL. The output of the 2:1 multiplexer can be either D_DELAYED or D, depending on the logic status of S, the output the CCM/DCM detector circuit which is controlled under the output signal (V_OFFTIME) of the zero current detector (ZCD). The UP and DW, the output of the charge pump circuit are decided by the phase difference between the output signal (D) of the hysteresis comparator and the output signal from the clock generator with the oscillation frequency of 2 MHz to be fixed. The role of the delay time control circuit is to be able to adjust the switching frequency with respect to the reference clock frequency.

The CCM/DCM selection circuit is composed of a CCM/DCM detector and a 2:1 multiplexer circuit. The CCM/DCM detector circuit consists of a comparator and logic circuits. The CCM/DCM detector circuit receives the output signal (V_OFFTIME) of ZCD and determines the status of the logic S to separate CCM from DCM. The output of the 2:1 multiplexer and the output of the ZCD
are able to control the output pulses, \( Q_P \) and \( Q_N \) of the dead time control circuit and buffer, so that \( Q_P \) and \( Q_N \) is capable of driving both the n-channel power switch (\( M_N \)) and the p-channel power switch (\( M_P \)). Depending on \( Q_P \) and \( Q_N \), the drain node of the power switches (\( M_N \) and \( M_P \)) can be connected to either the input signal, \( V_{IN} \) or the ground. The drain node of the power switches (\( M_N \) and \( M_P \)) is connected to both the power inductor (\( L \)) and the ZCD. The operation of the proposed converter is as follows. The converter can be either in DCM mode or in CCM, depending on the magnitude of the load current. If the load current becomes less than the threshold current which is 50 mA in this design, the overall circuit becomes in the DCM mode. As the output logic status (\( S \)) of the CCM/DCM detector becomes low (0), the 2:1 multiplexer selects the output signal (\( D \)) of the hysteresis comparator, so that the signal, \( D \) drives the power switches, \( M_P \) and \( M_N \). On the other hand, if the load current becomes greater than the threshold load current, \( S \) becomes high (1). The output signal of the hysteresis comparator enables the delay time control circuit to determine the delay time through the charge pump circuit and the compensation circuit.

The circuit diagram of the ramp generator circuit consisting of one multiplexer and one integrator (\( R_{ADD} \) and \( C_{FB} \)) is presented in Fig. 2. The multiplexer controlled by the \( Q_P \) signal on the p-channel power switch (\( M_P \)) generates a square waveform at node \( V_S \). The integrator with \( R_{ADD} \) and \( C_{FB} \) allows the square waveform (\( V_S \)) to be converted to the ramp signal. The ramp generator superimposes a ramp signal that becomes usually greater than that of the output ripple voltage onto the output ripple voltage at the input of the hysteresis comparator. This results in the switching frequency faster because the switching frequency becomes more dependent on the magnitude of ramp signal than the output ripple voltage. The parasitic values of the power filter such as ESR and ESL of \( C_o \) have negligible effect on the output voltage ripple and switching frequency [3].

The switching time period, \( T_S \) is described as (1).

\[
T_S = \frac{V_{IN} \cdot C_{FB} \cdot V_{HYST} \cdot R_{ADD}}{V_{OUT} \cdot (V_{IN} - V_{OUT})} \cdot T_D \cdot \frac{V_{IN}}{V_{OUT}} \cdot \frac{V_{IN}}{V_{OUT}}
\]

(1)

where \( V_{IN} \) and \( V_{OUT} \) are the input and output voltage of the buck converter, \( V_{HYST} \) is the window voltage of the hysteresis comparator, and \( T_{DEL1} \) and \( T_{DEL2} \) are the internal delay times of the switching on time and off time, respectively.

The delay time control circuit consists of PFD, charge pump and loop pass filter followed by the delay control cell shown in Fig. 3. The digital output of the hysteresis comparator \( D \) controls the switches M1 and M2 to charge capacitors C1 and C2 with current I1 and I2. The delay times \( T_{DEL1} \) and \( T_{DEL2} \) can be obtained by (2).

\[
T_{DEL1} = \frac{C_1}{I_1} \cdot V_{CTRL}, \ T_{DEL2} = \frac{C_2}{I_2} \cdot V_{CTRL}
\]

(2)
The output signal, \( D_{\text{DELAY}} \), of the delay time control circuit can be determined by the output of the S-R flip-flop which is controlled by the set signal, \( S \) and the reset signal, \( R \), where the reset signal is driven by the output of the AND gate of the S signal and the output of the comparator.

The PFD and the charge pump circuit detect the phase and frequency difference between the reference clock (CLK\(_{\text{REF}}\)) and the switching signal \( D \) to be able to adjust \( V_{\text{CTRL}} \). If the switching signal runs slower than CLK\(_{\text{REF}}\), the PFD will set DW signal to be high, so the capacitors in the compensation circuit will be discharged to reduce \( V_{\text{CTRL}} \). On the other hand, if the switching signal runs faster than CLK\(_{\text{REF}}\), the UP signal will become high, so the capacitors in the low pass filter will be charged to increase \( V_{\text{CTRL}} \). Because the delay times, \( T_{\text{DEL1}} \) and \( T_{\text{DEL2}} \) are directly proportional to \( V_{\text{CTRL}} \), the reduction of \( V_{\text{CTRL}} \) increases the frequency. This mechanism will make the switching frequency same as the frequency of the reference clock. [4] The fixed switching frequency obtained above is suitable for CCM and is not applicable to DCM.

### III. Measurement Results

The proposed buck converter was implemented by the 350 nm BCDMOS technology. The chip photograph is shown in Fig. 4. The effective die size of the proposed circuit is 1.37 mm x 1.37 mm, excluding the bonding pad and the power switches. The chip microphotograph of the delay time control circuit placed at the center of the chip is presented in Fig. 5.

As the load current varies from 50 mA to 450 mA, the simulated waveform of the \( V_{\text{CTRL}} \), \( V_{\text{OUT}} \) and \( S \), the output of CCM/DCM detector are presented in Fig. 6. When the load current becomes larger than 50 mA, the S becomes logic ‘1’ and the switching frequency becomes 2.0 MHz which is exactly the same as the measured frequency in CCM. When the load current becomes smaller than 50 mA, the S becomes logic ‘0’ and the switching frequency becomes 1.6 MHz in DCM. The switching frequency in DCM was measured to be 1.81 MHz. There is a discrepancy in DCM between the simulated and measured switching frequency due to the corner variation of the process. The output ripple voltages with the load currents, 50 mA, 250 mA, 350 mA, and 450 mA are simulated to be less than 5.5 mV. The minimum load current of 50 mA can be lowered within the threshold current of the CCM/DCM detector circuit.

The average output DC voltage, output ripple voltage, and switching frequency with the load current of 300 mA
shown in Fig. 7 were measured to be 1.21 V, 20 mV, and 2 MHz, respectively. The measured waveform in the bottom of Fig. 7 illustrates the waveform of the inductor input signal, $V_X$. The duty cycle of $V_X$ was measured to be 35%. The similar measurement results for the output DC voltage and output ripple voltage were obtained with the other load currents ranging from 100 mA to 450 mA. The measured switching frequency stayed at 2 MHz regardless of the various load currents. It proved that the proposed delay time control circuit enabled the proposed buck converter in CCM to fix the switching frequency of 2 MHz.

The maximum power efficiency of the proposed hysteretic buck converter was measured to be about 93% in Fig. 8. Comparison of the performances of the proposed work with the conventional works [5, 6] was made in Table 1. The switching frequency of the proposed work with both light load and heavy load were measured to be constant (1.8 MHz in DCM and 2.0 MHz in CCM) and to be higher than that of the conventional ones. The output ripple voltage of the proposed work was measured to be 20 mV, which is larger than that of the conventional ones. However, the fixed switching frequency does not cause EMI noise and using of the low value inductor makes the circuit smaller.

As the input or output voltage varies, the switching frequency stays constant because of the PLL architecture within the circuit as long as the circuit remains in the CCM mode with the clock frequency fixed.

### IV. Conclusions

This paper describes the proposed hysteretic buck converter for mobile applications. The proposed delay time control circuit enabled the proposed buck converter to achieve the measured switching frequency of 1.8 MHz in DCM and 2.0 MHz in CCM. The proposed circuit employs the ramp generator to be able to increase the switching frequency and delay time through the PLL structure. The proposed circuit was implemented by the 350 nm BCDMOS process. The effective chip size is 1.37 mm x 1.37 mm, excluding the bonding pad and power switches. The maximum efficiency of the proposed circuit was measured to be 93%. The measurement results demonstrated that the proposed hysteretic buck converter was capable of operating at a constant switching frequency of 2 MHz regardless of the load current varying from 50 mA to 450 mA. The magnitude of the minimum load current, which is the threshold of the CCM/DCM detector circuit can be changed.

| Table 1. Comparison of the performance of the proposed work with the conventional ones |
|----------------------------------|--------|--------|--------|
| Fs (light load)                  | 50 kHz | 670 kHz | 1.6 MHz |
| Fs (heavy load)                  | 1.38 MHz | 1.2 MHz | 2.0 MHz |
| Inductor                         | 10 uH  | 4.7 uH  | 1.2 uH |
| Capacitor                        | 20 uF  | 4.7 uF  | 15 uF  |
| $V_{IN}/V_{OUT}$                 | 2.7~4.2 V/2 V | 2.5~3.6 V/1.5 V | 3.7 V/1.2 V |
| Ripple voltage                   | 5.73 mV | 4.63 mV | 20 mV  |
| Load range                       | 50~500 mA | 20~600 mA | 50~500 mA |
| Transient response/overshoot     | 8.26 us | 79 mV  | N/A    | 5.5 us  |
| Efficiency                        | 89~95% | 88.7~96.4% | 90~93% |
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