Design of a Wide-Frequency-Range, Low-Power Transceiver with Automatic Impedance-Matching Calibration for TV-White-Space Application

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Abstract—This paper presents a wide-frequency-range, low-power transceiver with an automatic impedance-matching calibration for TV-white-space (TVWS) application. The wide-range automatic impedance matching calibration (AIMC) is proposed for the Drive Amplifier (DA) and LNA. The optimal S₂₂ and S₁₁ matching capacitances are selected in the DA and LNA, respectively. Also, the Single Pole Double Throw (SPDT) switch is integrated to share the antenna and matching network between the transmitter and receiver, thereby minimizing the systemic cost. An N-path filter is proposed to reject the large interferers in the TVWS frequency band. The current-driven mixer with a 25% duty LO generator is designed to achieve the high-gain and low-noise figures; also, the frequency synthesizer is designed to generate the wide-range LO signals, and it is used to implement the FSK modulation with a programmable loop bandwidth for multi-rate communication. The TVWS transceiver is implemented in 0.13 μm, 1-poly, 6-metal CMOS technology. The die area of the transceiver is 4 mm x 3 mm. The power consumption levels of the transmitter and receiver are 64.35 mW and 39.8 mW, respectively, when the output-power level of the transmitter is +10 dBm at a supply voltage of 3.3 V. The phase noise of the PLL output at Band 2 is -128.3 dBc/Hz with a 1 MHz offset.

Index Terms—TVWS transceiver, automatic impedance-matching calibration, drive amplifier, SPDT, N-path filter, LNA, phase-locked loop (PLL)

I. INTRODUCTION

The TV White Space (TVWS) is the DTV frequency band that is not used by the broadcasting companies to avoid inter-channel interference. This frequency band, however, can be used for useful applications besides the broadcasting purpose whereby the insufficient frequency resource is compensated for.

Fig. 1(a) shows the conception of the “TV White Space System,” and its standardization has been processed in an IEEE 802.15.4g working group [1]. The frequency band of the TVWS system is from 470 MHz to 698 MHz, as shown in Fig. 1(b).

Table 1 shows a frequency band of the TVWS PHYs. The frequency band of the TVWS application can be divided into the following three bands: Bands 1, 2, and 3 with total frequency ranges from 380 MHz to 928 MHz [1]. The TVWS transceiver should support such a wide frequency range with the following three data rates: 50 kbps, 150 kbps, and 200 kbps.

The TVWS transceiver needs to cover the wide frequency range of 380 MHz to 928 MHz and reject the large interferers due to the broadcasting signals. The TVWS transmitter is based on Frequency Shift Keying (FSK) modulation and involves a simple system architecture.

When low-power sensor networks are used in poor

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transmission environments, the output power should be controlled efficiently.

The required specifications of TVWS systems stipulate that the transmitted-power level must remain at an average of +10 dBm with a tolerance from -3 dB to 0.8 dB [1]. A Phase-Locked Loop (PLL) is used to implement the FSK modulator, and is directly modulated by varying the division value of the feedback divider with the output of the additional $\Sigma$-$\Delta$ modulator [2]. The VCO and divider in the PLL therefore need to have a wide operating-frequency range.

The drive amplifier (DA) should provide the high output power that minimizes the extent of a spurious emission over the wide frequency range. The automatic wideband-matching calibration is proposed and implemented in the DA to automatically select the optimal matching components depending on the channel frequency. The filtering characteristics of the DA can also be improved with the use of the automatic impedance-matching calibration.

In the receiver, the frequency characteristics of the input matching of the low-noise amplifier (LNA) should be wide, and the large interferers in adjacent channels should be rejected sufficiently. The tunable bandpass filter (BPF) is therefore needed to cover the wide frequency range of 380 MHz to 928 MHz. An on-chip N-path filter is designed to reject the large interferers in the adjacent channels. By using external inductors, the proposed system is advantageous compared to the previous works in terms of the area, cost, and power consumption.

In this paper, the wide-frequency-range TVWS transmitter, PLL, and receiver are all implemented by using the PLL with the programmable loop bandwidth to meet the low-power requirements.

### II. ARCHITECTURE OF TVWS TRANSCIEVER

Fig. 2 shows the block diagram of the proposed TVWS transmitter and receiver. It is composed of the PLL, a transmitter, and a receiver. The PLL is composed of a phase frequency detector (PFD), charge pump (CP), loop filter, VCO, local oscillator (LO) driver, delta-sigma modulator (DSM), and fractional-N divider. The transmitter is composed of a DA and an FSK modulator. Lastly, the output of the LO driver is connected to a DA to drive the transmitter antenna.

The receiver is composed of an SPDT switch, an LNA, a mixer, and a baseband. The SPDT switch is integrated to share the antenna and matching network between the transmitter and receiver, thereby minimizing the systemic cost. Also, the STD LNA with the mismatched calibration is designed to provide a high common-mode rejection and IIP3. The active-RC BPF with a programmable bandwidth is designed to support the data rates of 50 kbps, 150 kbps, and 200 kbps. The capacitors in each data rate are shared efficiently to minimize the die area.

As shown in Fig. 2, the proposed FSK transmitter with the PLL has data rates of 50 kbps, 150 kbps, and 200 kbps; in accordance with the IEEE 802.15.4g standard, the TX data is determined from the FSK-modulation data rate. Through the FSK modulator, the FSK_MOD signal becomes “0” or “1” in accordance with the TX data and is transferred to the modulation filter.
The modulation filter inputs the channel signal $I_F<17:0>$ and the $M_F<8:0>$ signal that are decided by the data rate. According to the FSK_MOD signal, the modulation filter adds or substrates $M_F<8:0>$ from $I_F<17:0>$.

Through the mapping of the value and filtering, the digital signal $O_F<17:0>$ becomes the output of the modulation filter and the DSM input signal. The DSM generates digital-control bits to adjust the division ratio of the fractional-N divider. The fractional-N division ratio is determined by the output of the digital-control DSM bits.

When the output frequency from the VCO and divider becomes the input of the fractional-N divider, the integer dividing ratio is decided by $PC<5:0>$ and $SC<3:0>$, and the fractional dividing ratio is decided by the $C<3:0>$ signal.

The selected fractional-dividing ratio through $O_F<17:0>$ changes the output frequency from VCO and the LO generator to approximately $+/-$ Fdev. When in the TX mode, the changed frequency becomes the input-TX input signal of the DA and the signal is modulated according to the data rate. When in the Rx mode, the selected channel frequency becomes the input Rx_I, Rx_Q signal of the mixer, and the channel is selected according to the data rate.

The proposed FSK transmitter with the PLL has data rates of 50 kbps, 150 kbps, and 200 kbps. In accordance with the IEEE 802.15.4g standard, the TX data is determined from the FSK-modulation data rate. Through the FSK modulator, the FSK_MOD signal becomes “0” or “1,” according to the TX data, and is transferred to the modulation filter.

As shown in Fig. 2, the proposed TVWS receiver is designed with a low intermediate-frequency (IF)-receiver structure and has an IF frequency of 200 kHz. The Rx-matching network is selected as the receiver path in the SPDT switch when a signal is received from the antenna of the 50 Ω Rx-matching network; the Rx-input signal is applied to the LNA without any reflection loss. The LNA amplifies a single signal by selecting either the high-gain or low-gain mode. The amplified single signal has a differential output through an STD structure.

The mixer has the LNA_I signal and LNA_Q signal as input signals, while the channel frequency has the Rx_I signal and Rx_Q signal as input signals. By mixing the I

![Fig. 2. The block diagram of the proposed TVWS transceiver.](image-url)
and Q signals from the LNA and PLL, the 200 kHz IF frequency is converted and transferred to the baseband.

The current-driven mixer is designed to improve the linearity performance over the wide frequency range. The N-path filter and current-driven mixer get four-phase LO signals from the 25% duty LO Generator.

The Duty Cycle Corrector (DCC) is designed to guarantee a duty ratio of 50% in the input signal of the 25% duty LO Generator.

The target sensitivity and maximum signal level of the receiver are –100 dBm and ~20 dBm, respectively; therefore, the gains of the LNA, tunable BPF, mixer, and base are controlled automatically to support the wide input dynamic range. The total gain control range is 68 dB and the total noise figure is 3.84 dB.

Since the frequency band is wide, the characteristics can be varied in accordance with the channel. Therefore, the calibration should be done each the channel switching. However, not all blocks don’t need the calibration, except for the baseband because the IF frequency is maintain with channel change. However, DA, LNA, and PLL should be calibrated according to channel switching. The specification of channel switch time is less than 200 us and the calibration time for the above blocks is within about 100 us. Therefore, the calibration with channel switching can be achieved within the specification time of channel switch.

The rejection for out band blocker would be determined by the RF/IF/baseband filter. The adjacent channel rejection specification is defined by the adjacent channel power. The Eq. (1) shows the attenuation requirements. The $P_{AN}$ means the allowable noise power.

$$\text{Attenuation}(@6\text{MHz}) \geq P_{\text{Blocker}} - P_{\text{AN}} \quad (1)$$

The $P_{\text{Blocker}}$ of TVWS specification is -20 dBm. If the $P_{\text{AN}}$ is assumed to -96 dBm, the attenuation at 6 MHz offset becomes more than 76 dB.

In order to satisfy the above specification, firstly, in RF frequency band, the N-path filter which bandwidth is 6 MHz rejects the blocker power and then the baseband attenuates as 100 dB/decade. Because the baseband is designed as a fifth order butter worth filter, blocker power can be suppressed sufficiently at 6 MHz offset from IF frequency as 200 kHz.

Fig. 3. The block diagram of the proposed drive amplifier.

### III. Circuit Description

#### 1. Driver Amplifier

Fig. 3 shows the block diagram of the DA in the transmitter. Since there are many interferers in the TVWS band, the wideband DA with the automatic impedance-matching calibration and tunable filter characteristics is proposed.

The center frequency of the DA is automatically tuned depending on the channel frequency. When the center frequency of the DA is shifted from the channel frequency, it can be automatically adjusted by the feedback loop and algorithm in Fig. 3.

The proposed DA is composed of a DA Core, Pre DA, Envelope Detector, 4Bit ADC, and Digital Logic. The Pre DA provides the gain and drives the DA Core, while the gain of the DA Core is controlled digitally. The proposed DA is also composed of four DA cells and the DA power gain is controlled digitally.

Fig. 4(a) and (b) shows the schematic of the Pre DA and DA Core, respectively.

Its filtering characteristics can be improved by the resonance at the selected frequency band using the load inductor.

The 5-bit capacitor bank is tuned by the control signals (P4 - P0) for wideband filtering characteristics. In addition, the negative Gm circuit has been added to compensate for the selectivity degradation that is due to the low-quality factor of the inductor.

To obtain a high power gain with a small DC current, a class-AB-type DA has been adopted; furthermore, a cascade-amplifier structure is adopted to guarantee stability by isolating the input and output under the high-output-power condition. The S22 parameter at the output of the DA Core can be adjusted by the control signals,
compensate for the output
(PVT) variation. To solve this problem, an AMC
text serious in terms of the process, voltage, and temperat

ture parallel, and the active DA power cells are controlled by
The cascode
S22_Cont<2:0>.

Fig.
130

The proposed LNA is of a single
chip spiral inductor is used as a load. Modeling
of the bond wire inductance, PAD capacitance, and
output matching networks are included in the simulation.
The cascode-based-DA power cells are connected in
parallel, and the active DA power cells are controlled by
the 4-bit control signal DA_CONT<3:0> to control the
output-power level.

2. Low Noise Amplifier (LNA)

The proposed LNA is of a single-to-differential (S to
D) conversion structure to reduce the cost, and the chip
size is minimized by eliminating the external elements.

But this structure has a fatal drawback because of the
mismatch of the differential output and this is more
serious in terms of the process, voltage, and temperature
(PVT) variation. To solve this problem, an AMC
(automatic mismatch calibration) loop is proposed to
compensate for the output-signal mismatch.

Fig. 5(a) shows the proposed S to D LNA-circuit
schematic that employs a compensatory AMC digital

block. This LNA is composed of a CG-CS-based balun-
topology attenuator that provides high-gain and low-gain
modes and a metal-oxide semiconductor (MOS) array. In
this CG-CS topology, M3 provides a 180-degree anti-
phase output (OUTB) [8]. An M2 transistor is used rather
than a resistor to resolve the voltage headroom, because a
resistor should be of a large value and size to reduce
thermal noise and it causes a large voltage drop [9];
however, this asymmetrical structure causes an output
mismatch and different parasitics. The output mismatch
induces an EVM (error vector magnitude) that affects
the unfavorable data-detection performance; but the
proposed method still requires a lower level of current
consumption than the conventional method and also
compensates for the output mismatch.

If the M3 PMOS transistor size is adjustable, the
current is also adjustable, meaning that the OUTB swing
level can also be controlled. The AMC loop is based on
SAR logic and senses the OUTB-node magnitude for
comparison with the OUT magnitude (reference value).
Therefore, the mismatch between OUT and OUTB can
be decreased despite of the frequency change.

3. Tunable Bandpass Filter and Current-Driven Mixer

Fig. 6 shows the block diagram of the tunable BPF.
The tunable BPF is an important block that is capable of
inhibiting the channel-interference characteristic at the
MOS.
tunable BPF was constructed using only a capacitor and a Duty Generator.

Atten. BPF is chosen when the small signal is transmitted from the LNA.

This case, however, the design cannot be fully implemented in a chip. This paper proposes the tunable BPF circuit design that has a high Q and does not require the use of an external inductor [11].

The tunable BPF has Mode <1:0> for the selection of the Attenuation mode (Atten. BPF) or P1dB mode. The Attenu. BPF is chosen when the small signal is transmitted from the LNA.

At this mode, the gain and attenuation characteristics are higher than those of the P1dB mode; alternatively, the P1dB mode is operated when a large signal is transmitted due to the higher performance of P1dB. The tunable BPF operates based on the 25% clock of the Duty Generator.

Fig. 7 shows the schematic of the tunable BPF. The tunable BPF was constructed using only a capacitor and MOS.

The tunable BPF was designed based on the structure of the N-path filter. The concept of the N-path filter is double mixing, whereby the first switch travels along a lower frequency, through the low-pass filter, and after the undesired signal is removed, it then returns back up to the original frequency by switching again. Since this circuit uses the divided phase for switching N paths, it is called the “N-path filter.”

Fig. 7 shows a tunable BPF circuit with 4 filter paths that have a 25% duty so that the phase is divided into 0°, 90°, 180°, and 270°.

The N-path filter is different from the conventional Gm-C filter. The center frequency of the proposed N-path filter is determined automatically, according to the switched frequency as LO frequency. Therefore, it is possible to automatically tracking the frequency without any control logic and signals.

Fig. 8(a) and (b) show the differential path circuit and the clock phases for the switches and the equivalent RLC circuit of the N-path filter, respectively [20]. The state equation from Fig. 8(a) is

\[ V_C(t) = V_C(nT_s + \sigma_3), \quad nT_s + \sigma_3 < t < (n+1)T_s \]  

(2)

where \( V_C(t) \) is the voltage on the capacitor in Fig. 8(a).

From the Fourier transform of the output in Eq. (3) based on Eq. (2), we can get final transform as Eq. (4).
We define notations of the switching frequency, N path filter -3dB bandwidth and duty cycle of each clock phase as \( f_s, f_{3\text{dB}}, \) and DT, respectively.

\[
V_{out,0}(f) = \sum_{n=0}^{\infty} H_n(f) V_{in}(f-nf_s) \tag{3}
\]

\[
H_n(f) = \frac{N}{1+ jf / f_{3\text{dB}}} \times (DT + \frac{1+\exp(j\pi(1-2DT)f / f_s)}{2\pi f_{3\text{dB}} / f_s}) \\
\times \left( \frac{\exp(j2\pi DTf / f_s) - \exp(-2\pi DTf / f_s)}{\exp(j2\pi / f_s) + \exp(-2\pi DTf / f_s) + 1/jf / f_{3\text{dB}} + (1-NDT)} \right) \tag{4}
\]

To improve the narrowband approximation, the poles of the switching frequency are considered. Equating the denominator of \( H_n(f) \) in Eq. (4) to zero to find the poles, as follows Eqs. (5, 6).

\[
\exp(s / 2f_s) + \exp(2\pi DTf / f_s) = 0 \tag{5}
\]

\[
s = 4\pi DTf_{3\text{dB}} \pm j2\pi f_s \tag{6}
\]

The high Q inductor can be obtained through the calculation of the N-path filter that can be represented by an equivalent-RLC-circuit model, as shown in Fig. 8(b).

The transfer function of the equivalent RLC circuit is shown as Eq. (7).

\[
H(s) = \frac{s / (RC)}{s^2 + (R + R_s)s / (R_s RC) + 1 / (LC)} \tag{7}
\]

The poles of the transfer function of the equivalent RLC circuit and N-path filter are equal.

As a result, the value of \( L \) in the RLC model is derived as Eq. (8) and we can verify the correlation between the Q and bandwidth mathematically according the R, C as Eqs. (9, 10).

\[
L = \frac{1}{4\pi^2 C(f_s^2 + 4(DTf_{3\text{dB}})^2)} \approx \frac{1}{C(2\pi f_s)^2} \tag{8}
\]

\[
BW = 1 / (2\pi (R / R_s)C) = 4DTf_{3\text{dB}} \tag{9}
\]

\[
Q = f_s / BW = f_s / f_{3\text{dB}} \tag{10}
\]

As the above formula, the smaller duty cycle switching is possible to obtain the high Q and the narrow band.

The larger the size of the switch is, the more favorable that the attenuation characteristics will be; however, the parasitic capacitance of the MOS switch causes a center-frequency offset. To reduce the frequency offset with a favorable attenuation characteristic, many phases are needed.

In this case, however, to build the edge of each of the phases, the current is indispensable. Since the current-driven mixer is based on the 4phase LO signal, the tunable BPF is also designed with a 4phase LO signal, and the frequency offset is reduced as much as possible to implement a 2stage and a dummy switch that has reversed phases with the main switch. This structure can remove the parasitic capacitance that occurs when the main switches are turned on.

Fig. 9 shows the RX_MIXER circuit diagram. The RX_MIXER mixes the RF signal that is amplified by the LNA, as well as the LO signal that is generated from the duty generator so that it changes to the IF signal; this architecture is operated based on the 25% duty cycle. In this paper, a passive type of mixer was used for the wideband. To compensate for the disadvantages of the passive-type mixer that has a low gain, a linear Gm cell and trans-impedance amplifier (TIA) were applied to obtain the high gain.

Fig. 10 shows the linear Gm cell. Since the cross-coupled cancels the \( 3^{\text{rd}} \)-order components, the linearity can be improved [12]; also, by using the complimentary and the corresponding Gm-boosting effect, a higher current gain can be obtained.
Fig. 9. Schematic of mixer.

Fig. 10. Schematic of linear Gm cell.

Fig. 11. Gain-control scheme of mixer.

Fig. 12. Timing diagram of 25% duty LO generator.

Fig. 13. Block diagram of LO Generator and 25% Duty Gen.

Fig. 14(a) shows the schematic of the DCC block. The DCC minimizes the variation of duty that occurs in the creation of the pulse wave from the divided-VCO output signal. The duty difference from the divided-VCO signal creates the offset between the VC+ and VC−, and the duty adjuster in Fig. 14(b) reduces the differential drive the current-driven mixer because a passive mixer has been adopted for the wideband transceiver. Since the mismatch of the duty and phase can affect the receiver performance, this block needs to be designed carefully.

Fig. 12 shows the timing diagram of the 25% duty LO generator. The 25% duty is generated by combining the 2LO and LO frequencies; the 2LO frequency is generated through the VCO division and the LO is created by dividing the 2LO signal. To create the 25% duty, the 2LO frequency and the 2LOB phase are critical factors; therefore, this paper proposes the duty cycle corrector (DCC) that is an analog-feedback method for precisely generating the 2LO signal.

Fig. 13 shows the block diagram of the LO generator and 25% Duty Gen. In RX mode, the 25% duty is generated by a gating between the 2LO and LO signals. The 2LO and 2LOB phases are optimized from the DCC, and the LO signal is generated by a division from the DCC [13].

4. 25% Duty LO Generator

The 25% duty generator (Duty Gen) is required to
5. Phase-Locked Loop

Fig. 15 shows a block diagram of the proposed PLL. The PLL is composed of a PFD, CP, loop filter, VCO, LO driver, and fractional-N divider. A coarse tuning, an automatic-phase-margin-compensation (APC)-loop circuit, and an automatic-amplitude-calibration (AAC)-loop circuit were adopted to maintain a constant frequency and output-voltage swing regardless of the PVT variation.

Moreover, the speed of the data signal for the data communication and the PLL lock time should be changed according to the different data rates (50 kbps, 150 kbps, and 150 kbps). To accomplish this, the proposed PLL automatically changes the PLL bandwidth according to the multi-data rate.

The APC-loop circuit automatically decides the PLL-loop bandwidth according to the data rate; however, from the PVT variation or other external circumstances, the PLL will be unstable. To solve this issue, the PLL-phase margin should be compensated from the APC loop. To control the loop bandwidth, the CP current, resistor, and capacitor of the loop filter are designed to be programmable. When the PLL-loop bandwidth is increased, the locking time is reduced; unfortunately, the wide bandwidth means that noise sources can translate into output jitter.

It is important that the PLL has a sound output-jitter performance after locking. The bandwidth-switching method is used to widen the loop bandwidth during the PLL locking operation and to narrow the loop bandwidth after the locking operation.

The bandwidth is switched to ensure a narrow value for the stable phase-locking operation, whereby the CP current, capacitor values, and resistor values are changed in the loop filter. If only the capacitor and resistor are changed for the bandwidth switching, a stability problem will occur. In this study, the CP current ICP is also controlled when the bandwidth is switched; as a result, the size variation of the capacitor and resistor can be reduced.

Fig. 16 shows the proposed schematic of wide band VCO, block diagram of the coarse tuning for the VCO and timing diagram of coarse tuning.

In order to improve the phase noise characteristics in wide band frequency, tunable LC filter and negative-gm are applied. The negative-gm attenuates the resistance of the inductor, so that Q factor can be enhanced. In addition, for phase noise, KVCO has the value as about 50 MHz/V.

The proposed wide range VCO can be implemented with cap bank control as VTRIM <7:0> of Fig. 16 through the coarse tuning.

The coarse tuning block can search the optimum capacitance value, VTRIM <7:0> to make the target frequency. The coarse tuning loop operates with the reference clock signal (REF_CLK) to generate RST_CNT, MSK_CNT, DEN_CLK, and COMP_CLK...
The VCO is detected through the 15-bit counter and is compared with the reference value (COMP_REF<14:0>). The frequency control signal (VTRIM<7:0>) is determined digitally based on the comparison result.

**IV. MEASUREMENT RESULTS**

The chip of the proposed system is implemented with a CMOS 0.13 μm process; Fig. 17 shows the chip microphotograph. The die area of the TVWS transceiver is 3,000 x 3,000 μm.

Fig. 18 shows the measured S22 results. The very wide TVWS band frequency is in the range of 470 MHz to 698 MHz; therefore, the S22 control bits (S22 Cont. <2:0>) are used by the DA block to match the control internally. By controlling the S22 Cont. <2:0>, the S22 wide matching is implemented under approximately -10 dB.

Fig. 19 shows the APC-loop transient-simulation results. The ED detects the Pre DA output swing and converts the swing to digital code <3:0> through the 4-bit ADC. The logic receives the ADC code <4:0> and then conducts a search to optimize the value of the Cap. Bank <4:0> code in order to find the max power of the DA.
When the power is optimized as max power, the logic does not work anymore and the Cap. Bank <4:0> code is fixed. Both the settling of the TX output at 10 dBm and the process of the Cap. Bank <4:0> search were observed. After the calibration, the Cal. Done signal is generated.

Fig. 20 shows the measured spectrum of the DA whereby the output power level is +10.17 dBm at a center frequency of 920.1 MHz.

Fig. 21 shows the measured TX-output-power level. The black line is the external control of the DA-block control bits by the SPI controller; the gray line is the APC-operation result. The power is maintained over 6 dBm. Also, the power value is similar between the external control and the APC.

Fig. 22 show the measured TX-output spurious emission at the minimum, center, and maximum frequencies of Band 2, respectively. Table 2 shows the specification of the spurious emission. Since only the TVWS band is used as a transceiver among the TETRA, TVWS, and ISM, the spurious-emission specification in the TVWS band should be checked. The specification shows that the proposed TVWS transceiver can meet the spurious-emission requirement.

Fig. 23 shows the AMC-loop transient-simulation results and comparison mismatch results between before and after AMC-loop. Before calibration, the voltage swings of the OUT and OUTB are 92.1 mV and 78.8 mV, respectively; however, both voltage-swing values become the same value after calibration, enabling the...
S11 control band frequency as LNA also needs to match decreased by 1.5% error range through the mismatch of LNA OUT and LNA OUTB is hard to obtain the same gain at all frequencies confirm Fig. 24 shows the measured S11 of the receiver. The V

Fig. 23. AMC-loop (a) transient-simulation result. (b) comparison mismatch percentage between before AMC and after AMC.

Fig. 24. Measured s11 of the receiver.

c confirmation of the compensation of the output mismatch.

Due to differential structure, LNA OUT and OUTB is hard to obtain the same gain at all frequencies. However, the mismatch of LNA OUT and LNA OUTB is decreased by 1.5% error range through AMC-loop.

Fig. 24 shows the measured S11 of the receiver. The LNA also needs to match the S11 at the same TVWS band frequency as the DA; therefore, the LNA has the S11 control bit (S11 Cont.<2:0>) with the Cap. bank

Fig. 25. Measured s11 of the LNA s21 and NF.

Table 3. The bandwidth results of the N-path filter

<table>
<thead>
<tr>
<th>Frequency</th>
<th>470 MHz</th>
<th>585 MHz</th>
<th>698 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3 dB BW simulation</td>
<td>4.65 MHz</td>
<td>5.74 MHz</td>
<td>6.44 MHz</td>
</tr>
<tr>
<td>-3 dB BW measurement</td>
<td>8.3 MHz</td>
<td>12 MHz</td>
<td>15 MHz</td>
</tr>
</tbody>
</table>

Fig. 26. Simulation result of tunable BPF (a) Noise figure, (b) S21 with measurement result.

<2:0>. By controlling the S11 Cont.<2:0>, S11 wide matching is achieved under approximately -10 dB.

Fig. 25 shows the measured S21 and NF of the LNA. The filtering characteristic is the most important factor of the TVWS transceiver; therefore, the front-end blocks need a filtering characteristic. In Fig. 28, we can see that the LNA maintains the overall gain and NF with the filtering characteristic in the TVWS band.

Table 3 shows the bandwidth results of the N-path filter both the simulation and measurement results.

Fig. 26 shows the S21 and NF results of the tunable
MHz and frequency and phase noise at Band 3 for ISM are 921.6 MHz and 575 MHz and frequency and phase noise at Band 2 are 383 MHz and respectively. The TVWS center frequency and phase noise at Band 1 are 383 MHz and respectively. Also, the frequency synthesizer is designed to achieve the high noise figure and LNA, and the optimal S22 and S11 matching capacitances are selected in the DA and LNA, respectively. Also, the SPDT switch is integrated to share the antenna and matching network between the transmitter and receiver, thereby minimizing the system cost. An N-path filter is proposed to reject the large interferers in the TVWS frequency band. A current-driven mixer with a 25% duty LO generator was designed to achieve the high-gain and low-noise figures. Also, the frequency synthesizer was designed to generate the wide-range LO signals and is used to implement the FSK modulation with a programmable-loop bandwidth for multi-rate communication.

The TVWS transceiver is implemented in 0.13 μm, 1-poly, 6-metal CMOS technology. The die area of the transceiver is 3 mm x 3 mm. The power-consumption levels of the transmitter and receiver are 64.35 mW and 39.8 mW, respectively, when the output-power level of the transmitter is 10 dBm at a 3.3 V supply voltage. The phase noise of the PLL output at Band 2 is -128.31 dBc/Hz with a 1 MHz offset. Table 4 is a summary of the measured performance of the TVWS transceiver.

### Table 4. Measured-performance summary of TVWS transceiver

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Technology</td>
<td>0.13 μm CMOS</td>
</tr>
<tr>
<td>Maximum Data Rate</td>
<td>200 kbps</td>
</tr>
<tr>
<td>Tx Output Frequency</td>
<td>470 MHz to 698 MHz</td>
</tr>
<tr>
<td>Phase Noise (@ Offset Frequency)</td>
<td>-128.31 dBc/Hz</td>
</tr>
<tr>
<td></td>
<td>(@ 1 MHz)</td>
</tr>
<tr>
<td>Output Power</td>
<td>+10 dBm</td>
</tr>
<tr>
<td>Total Tx Current (including PLL and Drive Amp)</td>
<td>64.35 mA @ +10 dBm Output</td>
</tr>
<tr>
<td>Total Rx Current</td>
<td>39.8 mW</td>
</tr>
<tr>
<td>Die Area</td>
<td>12 mm²</td>
</tr>
</tbody>
</table>

### V. CONCLUSIONS

This paper presents a wide-frequency-range, low-power transceiver with an automatic impedance-matching calibration for TVWS application. The wide-range automatic-matching circuit is proposed for the DA and LNA, and the optimal S22 and S11 matching capacitances are selected in the DA and LNA, respectively. Also, the frequency synthesizer was designed to achieve the high-gain and low-noise figures. The wide-range LO signals and is used to implement the FSK modulation with a programmable-loop bandwidth for multi-rate communication.

The TVWS transceiver is implemented in 0.13 μm, 1-poly, 6-metal CMOS technology. The die area of the transceiver is 3 mm x 3 mm. The power-consumption levels of the transmitter and receiver are 64.35 mW and 39.8 mW, respectively, when the output-power level of the transmitter is 10 dBm at a 3.3 V supply voltage. The phase noise of the PLL output at Band 2 is -128.31 dBc/Hz with a 1 MHz offset. Table 4 is a summary of the measured performance of the TVWS transceiver.

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