Sub-10 nm Ge/GaAs Heterojunction-Based Tunneling Field-Effect Transistor with Vertical Tunneling Operation for Ultra-Low-Power Applications

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Abstract—In this paper, we propose a sub-10 nm Ge/GaAs heterojunction-based tunneling field-effect transistor (TFET) with vertical band-to-band tunneling (BBT) operation for ultra-low-power (LP) applications. We design a stack structure that is based on the Ge/GaAs heterojunction to realize the vertical BBT operation. The use of vertical BBT operations in devices results in excellent subthreshold characteristics with a reduction in the drain-induced barrier thinning (DIBT) phenomenon. The proposed device with a channel length ($L_{cb}$) of 5 nm exhibits outstanding LP performance with a subthreshold swing ($S$) of 29.1 mV/dec and an off-state current ($I_{off}$) of $1.12 \times 10^{-7}$ A/μm. In addition, the use of the high-$k$ spacer dielectric HfO$_{2}$ improves the on-state current ($I_{on}$) with an intrinsic delay time ($\tau$) because of a higher fringing field. We demonstrate a sub-10 nm LP switching device that realizes a good $S$ and lower $I_{off}$ at a lower supply voltage ($V_{DD}$) of 0.2 V.

Index Terms—Tunneling field-effect transistor (TFET), low-power (LP) performance, short-channel effect (SCE), Ge/GaAs heterojunction, vertical tunneling operation

I. INTRODUCTION

For several decades, there have been rapid developments in the area of nano-scale electronic devices, and the miniaturization of devices has increased the density and speed of integrated circuits (ICs) and systems. To satisfy the increasing need for low-power (LP) consumption and low supply voltage ($V_{DD}$) increases in LP applications, devices are required to have excellent subthreshold characteristics. Conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) are unable to have subthreshold swing ($S$) below 60 mV/dec because of physical limitations and their principle of operation. Further, for short channel MOSFETs, it is difficult to decrease the subthreshold current because of drain-induced barrier lowering (DIBL) as one of the short-channel effect (SCE). Recently, tunneling FETs (TFETs) have been considered as promising candidates for next-generation LP devices because TFETs that are based on band-to-band tunneling (BBT) operations can realize attractive advantages such as lower off-state current ($I_{off}$) and superior $S$ [1-5]. However, as the channel length ($L_{cb}$) decreases below 10 nm, $S$ and $I_{off}$ values of TFETs are degraded drastically because of the drain-induced barrier thinning (DIBT) phenomenon, as well as direct tunneling between the source and drain, which is caused by the SCE in TFETs [6, 7]. Therefore, it is difficult for conventional TFETs with $L_{cb}$ values below 10 nm to obtain outstanding LP performance, and a novel structure and TFET operation principle is required to realize a sub-10 nm LP device.
In this work, we propose and examine a Ge/GaAs heterojunction-based TFET with a vertical tunneling operation to realize a good sub-10 nm LP device. To evaluate the LP performance, we obtain device characteristics such as $S$, $I_{off}$ and DIBT, and we also compare and analyze the values obtained using a conventional TFET. Moreover, we investigate the effect of spacer dielectrics on the vertical tunneling current in order to improve current performance and intrinsic delay time ($\tau$).

II. DEVICE STRUCTURE AND DESIGN

Fig. 1 shows a schematic cross section of the proposed device structure. The proposed structure is a stack structure consisting of Ge and GaAs layers. A high-quality Ge/GaAs heterojunction layer can be formed by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) systems because of a small lattice mismatch. The Ge/GaAs heterojunction has advantages in terms of the on-state current ($I_{on}$) of TFET. The lower energy band-gap ($E_g$) and lower electron effective mass ($m_e^*$) of the Ge material can increase the tunneling current with a high tunneling rate [8, 9]. In addition, because the GaAs material has a higher electron mobility, this property can also augment $I_{on}$ by improving the drift current [10]. The thicknesses of the Ge layer ($t_{Ge}$) and GaAs layer ($t_{GaAs}$) are 6 nm and 4 nm, respectively. The doping concentrations of the Ge layer ($n_{Ge}$) and GaAs layer ($n_{GaAs}$) are $5\times10^{19}$ cm$^{-3}$ (p-type) in the source and channel regions, and $1\times10^{18}$ cm$^{-3}$ (n-type) in the drain region. Further, the doping concentrations of the GaAs layer are $5\times10^{19}$ cm$^{-3}$ (n-type) in the channel region and $1\times10^{18}$ cm$^{-3}$ (n-type) in the source and drain regions. The channel doping concentrations were designed such that they increase the vertical tunneling probability that exists between the p-type Ge and n-type GaAs channel layers. The gate insulator with a thickness ($t_{ox}$) of 2 nm and the spacer dielectric consist of hafnium oxide (HfO$_2$), which enhances the current performances because of a higher gate controllability.

We obtained device performance by using the device simulator SILVACO ATLAS [11]. To increase the simulation accuracy, we applied various models including non-local BBT, Shockley-read-hall (SRH) recombination, and trap-assisted tunneling (TAT). The application of the TAT model is significant when simulating TFETs because the subthreshold characteristics of TFETs are influenced by the TAT mechanism that takes place through the trap or defect states in materials [12, 13].

III. RESULTS AND DISCUSSION

Fig. 2 shows the transfer characteristics of the proposed devices with different $L_{ch}$ values at a $V_{DS}$ of 0.2 V depending on the tunneling component.

Fig. 1. Schematic cross-section of the proposed device structure.

![Fig. 1. Schematic cross-section of the proposed device structure.](image1)

![Fig. 2. Transfer characteristics of the proposed device with different $L_{ch}$ values at a $V_{DS}$ of 0.2 V depending on the tunneling component.](image2)
place through the thin tunneling barrier. The transfer curve for the vertical tunneling current shows excellent subthreshold characteristics although $L_{ch}$ is reduced to 5 nm because the vertical tunneling mechanism is unaffected by DIBT. As $L_{ch}$ decreases, the vertical tunneling current decreases slightly because the tunneling area is involved in $L_{ch}$. In order to confirm accurately the effect of $L_{ch}$ on the vertical tunneling current, the onset voltage for devices with different $L_{ch}$ has been designed as a $V_{GS}$ of 0 V by controlling a metal gate work-function. In terms of lateral tunneling, the transfer curves show lower current performance. As shown in Fig. 3(b), lateral tunneling takes place because of the BBT between the p⁺ Ge channel and the n⁻ Ge drain regions. As $V_{GS}$ increases, the tunneling barrier between the p⁺ Ge channel and the n⁻ Ge drain regions becomes thinner because of fringing field, and the thinning of the tunneling barrier increases lateral current. However, when a high $V_{DS}$ is applied, lateral current at off-state increases because lateral tunneling barrier is influenced by $V_{DS}$. In other words, lateral tunneling operation is affected by DIBT phenomenon. Thus, in order to minimize the lateral tunneling current with DIBT phenomenon, we designed the device such that is has a lower doping concentration in the Ge drain region. As a result, the proposed device obtained a lower lateral current at both on- and off-state because the tunneling barrier is increased by the lower doping concentration in the Ge drain region. Fig. 4 shows the transfer curves of the proposed device and a conventional TFET. For comparison with the proposed device, we designed the conventional TFET as a Ge/GaAs heterojunction-based nanowire structure with an $L_{ch}$ value of 5 nm and $t_{ox}$ of 2 nm. We chose a nanowire structure to minimize the SCE with a higher gate controllability. The doping concentrations of the Ge source, GaAs channel, and GaAs drain regions are $5 \times 10^{19}$ (p-type), $1 \times 10^{16}$ (p-type), and $5 \times 10^{18}$ cm⁻³ (n-type), respectively. The transfer characteristic of the conventional TFET exhibits a higher $I_{off}$ and more degenerated $S$ compared to that of the proposed TFET. This result indicates that the subthreshold characteristics of the conventional TFET are degraded because of tunneling between the source and drain regions, which is caused by the thin channel layer. On the other hand, the proposed TFET exhibited excellent subthreshold characteristics because although $L_{ch}$ is 5 nm, the dominant tunneling current in the

Fig. 3. (a) Energy band diagrams in the Ge and GaAs channel regions, (b) Energy band diagrams in the Ge channel and Ge drain regions at on- and off-states. Energy band diagrams are extracted following the A-A' and B-B' line in Fig. 1(a).

Fig. 4. Transfer curves in the proposed TFET and the conventional TFET with a nanowire structure. Both devices are designed as Ge/GaAs heterojunction-based structures with an $L_{ch}$ value of 5 nm and $t_{ox}$ of 2 nm.
The proposed TFET is the vertical tunneling operation. Fig. 5(a) shows a comparison of $S$ and DIBT for the proposed TFET and the conventional TFET as a function of $L_{ch}$. We obtained $S$ as the inverse slope between the point of the off-state voltage and the point of the threshold voltage ($V_{th}$) in the transfer curve and defined $V_{th}$ as $V_{GS}$ for a drain current ($I_{DS}$) of $10^{-7}$ A/μm. We also obtained DIBT by finding the rate of change of $V_{th}$ when $V_{DS}$ was within the range of 0.2 V and 0.05 V [6]. While the values of $S$ and DIBT in the conventional TFET increased dramatically as $L_{ch}$ decreased from 15 nm to 5 nm, the corresponding values in the $S$ and DIBT in the proposed TFET exhibited small changes because of the vertical tunneling operation. The value of $S$ in the proposed device increased slightly, and this was due to a reduction of vertical tunneling area. The proposed TFET for an $L_{ch}$ of 5 nm has a higher $I_{on}/I_{off}$ ratio of $1.27 \times 10^7$ with a lower $I_{off}$, as shown in Fig. 5(b). These characteristics demonstrate the superiority of the proposed device for LP performance.

Fig. 6(a) shows transfer curves for devices with the different spacer dielectrics SiO$_2$ and HfO$_2$. The device with spacer dielectric HfO$_2$ has a higher vertical and lateral tunneling current than that with SiO$_2$ because of a difference in the fringing field effect. The fringing field effect is dependent on the spacer dielectric, and a high

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**Fig. 5.** A comparison of device characteristics in the proposed TFET and the conventional TFET with a nanowire structure as a function of $L_{ch}$ (a) $S$ and DIBT, (b) $I_{off}$ and $I_{on}/I_{off}$.

**Fig. 6.** (a) Transfer curves, (b) simulated contour plots of electron vertical BBT rate of devices for different spacer dielectrics SiO$_2$ and HfO$_2$. 
The spacer dielectric permittivity increases the fringing field effect [14]. As shown in Fig. 6(b), the source-side spacer dielectric HfO$_2$ extended the vertical tunneling area because vertical tunneling between p$^+$ Ge and the n$^-$ GaAs source regions was occurred by the higher fringing field.

Therefore, the device with HfO$_2$ has an enhanced vertical tunneling current. In terms of the lateral tunneling, the high fringing field also results in an increase in the lateral tunneling current by lowering the energy band in the drain region.

Fig. 7(a) shows the gate capacitances of devices with both SiO$_2$ and HfO$_2$. The device with HfO$_2$ realized the higher gate capacitance ($C_{gg}$) with an increase in the gate-to-drain capacitance ($C_{gd}$) and gate-to-source ($C_{gs}$). $C_{gs}$ is the total gate capacitance as a sum of $C_{gd}$ and $C_{gs}$. The increases in $C_{gs}$ and $C_{gd}$ were due to the higher permittivity in the spacer dielectric because high-$k$ spacer dielectrics increase the outer fringe capacitance ($C_{of}$) component [15]. Although the device with HfO$_2$ has the higher $C_{gg}$, we obtained a lower $\tau$ because of the higher current performance, as shown in Fig. 7(b). The value of $\tau$ is proportional to the value of $C_{gg}/I_{on}$ [16]. As a result, the device with HfO$_2$ exhibited a lower $\tau$ of 0.58 ps for a $V_{gs}$ of 0.5 V.

IV. CONCLUSIONS

We proposed a Ge/GaAs heterojunction-based short-channel TFET with vertical tunneling operation that has an excellent LP performance. The proposed device was unaffected by the impact of the DIBT phenomenon due to vertical tunneling operation. Moreover, by designing a high-$k$ spacer dielectric, we obtained an improved vertical tunneling current as well as a lower $\tau$. The proposed device with $L_{ch} = 5$ nm exhibited excellent characteristics, including an $I_{on}$ of 142 $\mu$A/μm, $S$ of 29.1 mV/dec, $I_{on}/I_{off}$ ratio of $1.27 \times 10^7$, and $\tau$ of 0.58 ps. We confirmed that the proposed device is suitable for ultra LP devices at $V_{DS}$ of 0.2 V.

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