Nano-Scale Cu Direct Bonding Technology Using Ultra-High Density, Fine Size Cu Nano-Pillar (CNP) for Exascale 2.5D/3D Integrated System

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Abstract: We propose nano-scale Cu direct bonding technology using ultra-high density Cu nano-pillar (CNP) with for high stacking yield exascale 2.5D/3D integration. We clarified the joining mechanism of nano-scale Cu direct bonding using CNP. Nano-scale Cu pillar easily bond with Cu electrode by re-crystallization of CNP due to the solid phase diffusion and by morphology change of CNP to minimize interfacial energy at relatively lower temperature and pressure compared to conventional micro-scale Cu direct bonding. We confirmed for the first time that 4.3 million electrodes per die are successfully connected in series with the joining yield of 100%. The joining resistance of CNP bundle with 80µm height is around 30 m for each pair of 10µm dia. electrode. Capacitance value of CNP bundle with 3µm length and 80µm height is around 0.6fF. Eye-diagram pattern shows no degradation even at 10Gbps data rate after the lamination of anisotropic conductive film.

Keywords: nano-scale Cu direct bonding, Cu nano-pillar, esascale 2.5D/3D integration

1. Introduction

In current high performance 2.5D field-programmable gate array (FPGA) product, a FPGA die has typically 50,000 electro-plated Cu/Sn bumps with 20 µm diameter and 45 µm pitch for joining to a Si interposer. However, ultra-scale 2.5D/3D FPGA requires ultra-high joining density of more than few millions per FPGA die in coming year. Moreover, ultra-high bandwidth memory (3D DRAM) and ultra-high density storage memory (3D Flash) also require ultra-fine joining pitch below 1 µm due to the limited region for TSV array in a die in a future. To meet such requirement, the bump size should be shrunken to 1 µm or sub-µm in diameter. Current standard electro-plated Cu/Sn bump has been scaled vertically and horizontally by increasing Cu volume and decreasing solder volume. However, it is difficult to scale the bump pitch below 5 µm in current electro-plated Cu/Sn bumping process, especially because of the shrinkage limitation of Sn volume. Some volume of Sn layer is required for solidable joining. However, Sn layer easily bridge with near bumps if the misalignment accuracy of the chip bonder is larger than 1 µm and if the bonding pressure is too high. Oxide direct and Cu/oxide hybrid bonding technologies have attracted attention as bump-less joining solution to overcome the scaling limitation of electro-plated Cu/Sn bump. Cu/oxide hybrid bonding technology is a more promising solution for ultra-high density 2.5D/3D integration applications, because oxide direct bonding has severe challenges such as the difficulty to etch very thick multilayer of dielectrics for through oxide via (TOV) and huge area penalty due to high density TOVs. However current standard chip-to-wafer (C2W) and wafer-to-wafer (W2W) hybrid bonding technologies have also many challenges such as difficulties to control the good post-CMP (chemical mechanical polishing) topography with no Cu dishing, height uniformity (global/local), surface roughness, CMP reproducibility in all Cu electrodes and the severe control of killer particle, surface oxide layer for gap-free intact bonding to achieve high stacking yield. In this paper, to overcome those issues and to achieve high stacking yield, we propose a novel hybrid bonding technology based on nano-scale Cu direct bonding using ultra-high density Cu nano-pillar (CNP) for exascale 2.5D/3D integration.

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To dramatically enhance the joining density with high stacking yield for exascale 2.5D/3D integration, we propose novel hybrid bonding technology using a scaled electrode structure (bump-less) and a unique adhesive layer compose of ultra-high density Cu nano-nail (CNP) as shown in Fig. 1. Target specification of scaled tiny electrode is sub-µm diameter and 1 µm pitch for ultra-high joining density of more than ten millions per die. This novel hybrid bonding technology has unique features; shallow extruded Cu electrode and unique adhesive layer of anisotropic conductive film compose of ultra-high density, fine size CNP. This scheme can avoid the critical challenges of current standard hybrid bonding process such as killer particle, roughness/height variations in all Cu electrodes across wafer/chip and consequentially achieve high stacking yield in tact bonding. Figure 2 show the conceptual process flow of novel hybrid bonding technology using ultra-high density CNP. Surfaces of incoming functional and interposer wafers with Cu electrodes and inter-metal dielectric (IMD) layers are simultaneously flattened by conventional chemical mechanical polishing (CMP) and post-cleaning. Then IMD layer is shallow-recessed around 100–300 nm in depth by damage-free plasma etch-back to form slightly extruded Cu electrode structure. The recessed IMD layer structure can mitigate the killer particle (sub-µm size) issue. To dramatically enhance the stacking yield, in this work, we introduce a unique adhesive layer of anisotropic conductive film comprising ultra-high density CNP and inorganic insulator. The anisotropic conductive film is transferred on the surface of wafer by conventional tape laminating process. After diced, chips bond to another wafer for chip-to-wafer (C2W) hybrid bonding approach. This hybrid bonding technology can be also applied to wafer-to-wafer (W2W) bonding approach as well, because the anisotropic conductive film can effectively compensate the wafer warpage. Figure 3 shows SEM cross-sectional images after Cu/oxide IMD CMP process (a) and after the etch-back of oxide IMD layer (b). Cu surface shows no severe dishing and good flatness to the oxide layer even by our conventional CMP & cleaning processes. Oxide layer is shallow recessed around 300 nm in depth by well-controlled plasma etch-back process.

In the anisotropic conductive film, Cu is filled into a large number of isolated nano-holes with 60 nm diameter and 100 nm pitch formed in anodized aluminum oxide (AAO) substrate. Figure 4(a) and (b) shows the conceptual structures of anisotropic conductive film compose of nano-Cu filaments and inorganic insulator, where (a) and
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Figure 4. The conceptual structure of top view (a) and bird view (b), and SEM top view (c) and cross-sectional view (d) of fabricated anisotropic conductive film comprising ultra-high density CNPs in AAO substrate.

(b) represent the top view and the bird’s-eye view, respectively. Figure 4(c) and (d) shows SEM images of the anisotropic conductive film with the top view and the bird’s-eye view, respectively. AAO is a well-known porous material, which is formed by electrochemical oxidation of aluminum in acidic solution. Figure 5 shows the fabrication process of anisotropic conductive film comprising ultra-high density, fine size CNP in the AAO substrate. The densely-arranged vertical pores with 60 nm diameter with 100 µm depth are formed spontaneously in an aluminum substrate by electrochemical oxidation in acidic solution. After remove the aluminum substrate, fine size nano-pores with 60 nm diameter in the AAO substrate with 100 µm thickness are completely filled by Cu (aspect ratio, 1660:1) without voids using well-controlled electrolytic plating method. Then, both surface of AAO substrate are polished to remove Cu metal and thinned down to the target thickness of conductive film around 10~80 µm. The planarization process is important to achieve the uniform thickness of CNP in the AAO substrate. The well-controlled wet etchant recesses slightly an aluminum oxide layer from the surface of AAO substrate to extrude CNP with the height of 0.1~0.5 µm. The tip height of CNP is controlled flexibly to compensate the height variation of

Figure 5. The fabrication process of inorganic anisotropic conductive film composed of ultra-high density CNP in alumina substrate.
Cu electrode caused by the planarization process. Finally, thin glue layer below 1µm thickness is coated on the surface of CNP to protect from the oxidation of Cu surface and to enhance the mechanical joining strength between wafer/chips. The electrical conductivity appears only in the vertical direction along filled Cu metal, and the excellent insulation property by AAO is obtained in the horizontal direction.

We assume that nano-scale Cu direct bonding using nano-size Cu pillar has different joining mechanism compared to current standard Cu-Cu direct bonding. Figure 6 shows the concept of joining mechanism based on nano-scale Cu direct bonding using ultra-high density CNP. Nano-scale CNPs intact-contact (slightly penetrate) to Cu electrode in chips at R.T. Then, CNPs bond with Cu electrode by re-crystallization due to the solid phase diffusion of Cu atoms between CNPs and Cu electrode and by morphology change of CNP to minimize interfacial energy at 250°C and relatively lower pressure. Nano-sized CNP can provide low temperature and low pressure Cu-Cu direct bonding. CNP easily contact into Cu electrode even if some residuals or thin oxide layer or particles remains on the surface of Cu electrode. Therefore, CNP provides high yield intact bonding.

Moreover, inorganic alumina dielectric in anisotropic conductive film gives high thermal conductivity and low coefficient of thermal expansion (CTE) value compared to conventional organic resin. Therefore, alumina substrate and ultra-high density CNP in the conductive film can be used as excellent thermal dissipation paths in 3D systems.


In order to evaluate the feasibility of new hybrid bonding technology using ultra-high density CNP, we fabricated TEG (Test Element Group) module. A TEG die size is 7 mm×23 mm aiming to 2.5D/3D high-end FPGA application. A TEG module composed of 4 TEG dies. The huge number of electrodes of 4.3 million (4,309,200) are formed...
in the each die, where the size and pitch of Cu electrode are 3 µm and 6 µm respectively. Figure 7 shows the fabrication process flow of TEG module by new reconfigured W2W hybrid bonding technology based on nano-scale Cu direct bonding using ultra-high density CNP. We fabricated 300 mm TEG wafer and interposer wafer with ultra-high density Cu electrode and plasma tetraethyl orthosilicate (P-TEOS) IMD layer in our 300 mm wafer 3D-LSI fabrication line. After Cu/oxide planarization by conventional CMP process, oxide IMD layer is shallow-recessed by plasma etch-back process. The anisotropic conductive film comprising ultra-high density CNP and alumina oxide substrate with 80 µm thickness is transferred on the surface of TEG wafer by conventional tape laminating process and then TEG wafer is diced. Multi-numbers of TEG chip are simultaneously assembled with high accuracy on the interposer wafer by chip self-assembly method using the surface tension of liquid and thermal-compression-bonded at 250°C in batch by the wafer gang bonder.

A bundle of CNP behaves as an electrode via to connect between top and bottom electrodes. Figure 11 shows the conceptual structure of bundle of CNP as an electrode via (a) and the joining resistance of CNP bundle (b), respectively. The CNP bundle size depends on the electrode size. A CNP bundle of 3 µm square size has total number of 900 CNPs with 60 nm size and 100 nm pitch. Electrical joining
area is around 30% in Cu electrode. Resistance of CNP ($R_{J1}$) is composed of two contact resistances ($R_{C,U}$, $R_{C,L}$) to both electrodes and one wire resistance ($R_{CNP}$). Figure 12(a) and (b) shows the I-V characteristics measured in the daisy chain of the TEG chip which is bonded by the non-optimized condition. All of 4,309,200 electrodes with 3 µm diameter are well connected which gives rise to the joining yield of 100% even the non-optimized condition. The joining resistance measured in the small unit daisy chain with 136,800 electrodes through 3 µm diameter CNP bundle comprising 900 CNPs was around 3W at 1V for each pair of joining as shown in Fig. 12(a). Both contact and wire resistances are included in this joining resistance. However, the joining resistance per each pair increases to around few hundred W at 1V when the number of electrodes in the daisy chain increases to 4,309,200 as shown in Fig. 12(b). Such a high resistance may indicate that parts of poor joining electrodes with higher resistance are included in the daisy chain with a larger number of electrodes. We assume that the poor joining is mainly induced by a non-uniform contact between electrode and CNPs. Therefore it is indispensable to eliminate these poor joining electrodes with higher resistance for further reducing the joining resistance. In order to dramatically decrease the joining contact resistance, we minimized the height variation of CNP in AAO substrate and Cu electrode on a wafer as much as possible by the optimized CMP process.

Figure 13 shows SEM cross-sectional image of fabricated TEG module after the optimization of height variation of CNP and Cu electrode. Anisotropic conductive film is thinned down to 20 µm thickness to improve the height variation of CNP. 10 µm square Cu electrode is used to minimize the misalignment affect. Figure 14 shows the I-V characteristics measured in the daisy chain of the TEG chip which was bonded by the optimized condition.

Fig. 11. Conceptual structure of bundle of CNP as a via (a) and joining resistance of CNP bundle (b).

Fig. 12. The I-V characteristics measured in daisy chains of the TEG chip which was bonded by the non-optimized condition; minimum unit of 136,800 electrodes (a) and 4,309,200 electrodes (b), respectively.

Fig. 13. SEM cross-sectional image of fabricated TEG module after the optimization of height variation of CNP and Cu electrode.

Fig. 14. The I-V characteristics measured in daisy chains of the TEG chip which was bonded by the optimized condition.

Fig. 15. The conceptual configuration of the coupling noise effect which may happen by neighbored ultra-high density CNP between electrodes.
The joining resistance is dramatically decreased to around 30–50 mW for each pair of joining at 1V.

However this bonding approach using ultra-high density CNP has a couple of potential reliability challenges. One of the potential challenges is the coupling noise effect which may happen by neighbored ultra-high density CNP between electrodes, they do not join the electrical connection as shown in Fig. 15.

We characterized the capacitance of CNP bundle using the TEG pattern. The TEG pattern is composed of Cu wire with 10 µm width, 1 µm thickness, and long wire lengths of 500/1000mm with the various spaces. The capacitance of CNP bundle is measured at before and after the lamination of anisotropic conductive film with 80 µm thickness as shown in Fig. 16. The capacitance value is normalized from the measured value using long wire length of 500 mm to exclude the effect of wire length. Figure 17 show normalized capacitance values of CNP bundle per wire length at without and with anisotropic conductive film. Normalized capacitance of CNP bundle (*C_{B,CNP}) is 0.2 fF per µm length. Therefore estimated capacitance value of CNP bundle with 3 µm length, 3 µm width and 80 µm height is around 0.6fF. This capacitance value may not induce severe cross-talk noising effect. To more reduce the capacitance of CNP bundle for high frequency application, thickness of conductive film should be shrinkage.

Fig. 16. The conceptual structure to evaluate capacitance and crosstalk of CNP bundle before (a) and after (b) the lamination of anisotropic conductive film, respectively.

Fig. 17. Normalized capacitance values of CNP bundle per wire length at without and with anisotropic conductive film.

We characterized the high frequency characteristics of anisotropic conductive film using the TEG pattern. Figure 18 show the configuration of TEG pattern (a) and the optical image of fabricated TEG pattern (b). The TEG pattern is composed of Cu wire of 1 µm thickness with various width, length, and space between Cu wires. Eye diagram is measured using the TEG pattern of 5 mm length, 8 µm space, and 3 µm width at before and after the lamination of anisotropic conductive film with 80 µm thickness using the same method as shown in Fig. 16. Eye-diagrams are compared at various data rate as shown in Fig. 19. Eye-diagram shows no degradation even at 10Gbps data rate after the lamination of anisotropic conductive film.

In this study, ultra-high density electrodes of 4.3 million per die is successfully intact-bonded with the 100% joining yield by new hybrid bonding technology based on nano-scale Cu direct bonding using ultra-high density CNP. The major advantage of our hybrid bonding technology is that it is tolerate for the process variations such as the height and thickness variations of Cu electrode, the flatness variation of Cu electrode and IMD layer, chip/wafer
Our hybrid bonding technology can give a promising solution for realizing high yield exascale 2.5D/3D integration even by using current standard CMP, post-cleaning, and bonding processes, because it is not necessary for severely controlling the critical challenges such as killer particles, residuals, oxide layer on electrode surface and morphology, roughness, height variation in all Cu electrodes. We will investigate the assembling process comparability and the potential reliability challenges by implementing the functional FPGA module.

4. Summary

We proposed nano-scale Cu direct bonding technology using ultra-high density Cu nano-pillar (CNP) for exascale 2.5D/3D integration. We clarified the joining mechanism of nano-scale Cu direct bonding using CNP. We confirmed for the first time that 4.3 million electrodes per die are successfully connected in series with the joining yield of 100%. The joining resistance of CNP bundle is around 30–50 mW for each pair of 10 µm electrode after the optimization of CNP height variation. Capacitance value of CNP bundle with 3 µm length and 80 µm height is calculated around to 0.6fF. Eye-diagram pattern shows no degradation even at 10Gbps data rate after the lamination of anisotropic conductive film.

References


