Third Harmonic Injection Circuit to Eliminate Electrolytic Capacitors in Light-Emitting Diode Drivers

Jin-Wan Yoo*, Kwang-Hyun Jung*, In-Ung Jeon* and Chong-Yeun Park†

Abstract – A new third harmonic injection circuit for light-emitting diode (LED) drivers is proposed to eliminate electrolytic capacitors and thereby extend the lifetime of LED drivers. When a third harmonic current is injected to the input current of the LED driver, the required capacitance of the driver can be reduced. The proposed circuit can control an injection ratio and has simple circuitry. The synchronous third harmonic is generated by a phase locked loop (PLL), a 1/3 counter, and op-amps and applied to a power factor correction circuit. Thus, the storage capacitor can install film capacitors instead of the electrolytic capacitor. The value of storage capacitance can be reduced to 78% compared to an input power factor of 100%. The proposed circuit is applied to the 80W prototype LED driver to experimentally verify the performances.

Keywords: LED, Electrolytic capacitor, Third harmonic injection circuit, PLL

1. Introduction

Since the power consumption of lighting has been increasing with rising demands, the reduction of lighting energy has become an important issue. The LED (Light Emitting Diode), a semiconductor component, not only has a higher luminance efficacy but also lasts longer, is environmentally friendly, and is smaller than conventional light sources. Thus, LEDs have been replacing conventional light sources [1-4].

One of the greatest advantages of LEDs is their extended lifetime. However, LED drivers have a shorter lifetime than LED chips because the electrolytic capacitors do not last 20,000 hours [5, 6]. Since most LED drivers require large capacitance, electrolytic capacitors are often used, especially for the PFC (Power Factor Correction) circuit’s output. PFC circuits require a storage capacitor, which has a large value of capacitance, for balancing between input power as the squared sine function and output power as the constant.

Therefore, the storage capacitance reduction methods have been studied to replace the electrolytic capacitor with the film capacitor to extend the LED driver’s lifetime [7, 8]. The third harmonic current injection, one of the capacitance reduction methods, has been studied and tested by implementing it on 2 stage PFCs and single stage PFCs [9-11]. This method has been implemented either using analog multipliers or a MCU (microcontroller-unit). However, these methods have problems which are high cost and low reliability respectively. And both are hard to control the third harmonic ratio.

Thus, in this paper, a new circuit is researched for the third harmonic injection with a PLL (Phase-Locked Loop). Then, the proposed circuit is applied to an 80W boost type PFC and tested. The third harmonic ratio is determined to satisfy the IEC-61000 class C by presenting the power factor and the THD (Total Harmonic Distortion) while controlling the ratio of the fundamental input current to third harmonic current. The first section presents a concept of the third harmonic injection method and then the new circuit. Subsequent sections include the experimental results and discussion.

2. Third Harmonic Injection Method

This section describes the third harmonic injection method to eliminate electrolytic capacitors, which decrease the lifetime of LED drivers.

2.1 Lifetime of components in LED lighting

LED chips have a lifetime of 100,000 hours; however, LED lighting has a shorter lifetime than LED chips because LED drivers consist of electrolytic capacitors. The lifetime of electrolytic capacitors can be calculated by Eq. (1).

\[ T = B \times 2^{\frac{T_0 - T_a}{10}} \]  

where B is the base lifetime, and \( T_0 \) is the maximum operating temperature, \( T_a \) is the current temperature. The lifetime of electrolytic capacitors, film capacitors, and LED chips is shown in Fig. 1.
As shown in Fig. 1, the high temperature decreases the capacitors’ lifetime. However, the film capacitor’s lifetime is more than 80,000 hours even at the 95°C ambient temperature, which is much a longer lifetime than the electrolytic capacitor [12]. In addition, the film capacitor has longer lifetime than the LED chip [13]. Consequently, if all capacitors of the LED driver are replaced with the film capacitor and there are no other components with a shorter lifetime than LED chips, the lifetime of the LED lighting will follow the LED chips. Thus, the electrolytic capacitor in the LED driver should be replaced with the film capacitor to extend LED lifetime.

2.2 Concept of the third harmonic injection method

The electrolytic capacitor is used to balance the sinusoidal input power and the DC output power. This capacitor is called a ‘storage capacitor,’ which is installed at the PFC output. Using the capacitance reduction method, the storage capacitor could be replaced by the film capacitor, which has a small capacitance.

The capacitance reduction method of distorting input current was verified by Barrado, Sanz, and Salas [7]. Especially, if the third harmonic is injected into the input current, required capacitance can be reduced by minimizing the difference between the input instantaneous power and the output power [8].

Fig. 2 shows the block diagram of the third harmonic injection by the boost type PFC.

With the assumption that the power factor is 1, key waveforms of the PFC can be represented as shown in Fig. 3.

Fig. 3. Key waveforms of the PFC for the unity power factor

The input voltage is presented in Eq. (2)

\[ v_{in}(t) = V_m \sin \omega t \]

(2)

As shown in Fig. 3, since the power factor is 1, the shape of the input current is formed as the input voltage. Therefore, the input current can be written as Eq. (3).

\[ i_{in}(t) = I_m \sin \omega t \]

(3)

Consequentially, the input power becomes Eq. (4).

\[ p_{in}(t) = V_m I_m \sin^2 \omega t = \frac{V_m I_m}{2} (1 - \cos 2\omega t) \]

(4)

Under the assumption that there are no power losses in the PFC circuit, the average input power can be presented as Eq. (5).

\[ P_{in} = \frac{V_m I_m}{2} = P_o \]

(5)

The capacity of the capacitor is related to variation of the energy and can be represented as Eq. (6).

\[ \Delta E = \frac{1}{2} C_b V_{p-p}^2 \]

(6)
As presented in Eq. (6), the storage capacitance is proportional to the \( \Delta E \). If the \( C_B \) is fixed, the \( \Delta E \) decreases according to the \( V_{ip} \) increase. On the other hand, if the \( V_{ip} \) is fixed, the required storage capacitance can be reduced. As shown in Fig. 3, since the \( C_B \) is charged during \( 1(T_{line})/8 \) to \( 3(T_{line})/8 \), the \( \Delta E \) can be written as Eq. (7).

\[
\Delta E = \int_0^{\frac{T}{8}} [p_{in}(t) - P_0]dt
\]

\[
= \frac{3T}{8} V_{m} I_m \left( 1 - \cos 2\omega t \right) - V_m I_m \frac{d}{dt} = \frac{P_0}{\omega} (7)
\]

Key waveforms of the PFC are illustrated in Fig. 4 when the third harmonic is injected into the input current [10].

If the third harmonic ratio is 35\%, the \( i_{in}(t) \) can be presented as Eq. (8) with the similar to Eq. (3).

\[
i_{in}(t) = I_m \sin \omega t + 0.35 I_m \sin 3\omega t \quad (8)
\]

Thus, using Eq. (8), the input power becomes Eq. (9).

\[
p_{in}(t) = V_m I_m \sin^2 \omega t + 0.35 \cdot V_m I_m \sin \omega t \cdot \sin 3\omega t
\]

\[
= V_m I_m \left( 1 - 0.65 \cdot \cos 2\omega t - 0.35 \cdot \cos 4\omega t \right) \quad (9)
\]

As shown in Fig. 4, since the \( C_B \) is charged during \( 3(T_{line})/32 < t < 13(T_{line})/32 \), the \( \Delta E \) is calculated as Eq. (10).

\[
\Delta E = \int_{\frac{3T}{32}}^{\frac{13T}{32}} \left[ p_{in}(t) - P_0 \right]dt
\]

\[
= \frac{3T}{32} \left[ V_m I_m (1 - 0.65 \cdot \cos 2\omega t - 0.35 \cdot \cos 4\omega t) - V_m I_m \right] \frac{d}{dt} = \frac{P_0}{\omega} (10)
\]

The result of Eq. (10) shows that the \( \Delta E \) value is 28\% less than Eq. (7). That means that 35\% of the third harmonic at the input current can reduce the storage capacitance to 72\%.

### 3. Design of the Third Harmonic Injection Circuit

The third harmonic injection can be achieved by relying on PFC operation. The boost type PFC forces the shape of the input current to adhere to the shape of the input voltage, which controls the frequency and duty cycle using the rectified input voltage, zero current detection, output voltage, and FET current sensing [14].

The distorted waveform of the input current can be achieved by inserting the combined waveform of the fundamental and the third harmonic injected into the reference input of the PFC.

Conventional circuits for the third harmonic injection are presented in Fig. 5. Since the first circuit includes two multipliers, the cost of the whole circuit could be high as shown in Fig. 5(a) [9]. Furthermore, third harmonic injection ratio is hard to control by first circuit. Another circuit produces the combined waveform of the fundamental and the third harmonic using MCU as shown in Fig. 5(b) [10]. This second circuit could have a simple circuitry. However, since the operation of the MCU is based on a clock, the impulsive noise could interrupt the operation or could skip the program counter. Thus reliability of the PFC circuit could be lower than the other analog circuits.

Thus, this paper proposes the third harmonic injection circuit to solve these problems. Fig. 6 shows the block diagram of the proposed third harmonic injection circuit with the boost type PFC.

The proposed circuit consists of a voltage sensing circuit, a comparator, a PLL, a band pass filter, an adder, and a rectifier.

It is critical that the third harmonic generator is synchronous to the input line’s fundamental frequency. The synchronization can be achieved using a PLL circuit. Fig. 7 shows the block diagram of third harmonic generator using a PLL.

The PLL with the 1/3 counter can produce the \( V_{PLL} \) which has three times the frequency of the \( V_{square} \). The phase detector has two inputs; one is the \( V_{square} \) for the reference frequency the other one is feedback from the 1/3
counter. The phase detector output changes as a result of the regulated DC level through the loop filter. The VCO (voltage-controlled oscillator) also oscillates three times faster than the \( V_{\text{square}} \) through the phase detector. As a result, a synchronous third harmonic can be generated through the input line voltage.

The key waveforms of the third harmonic generator are depicted in Fig. 8. The applied input line voltage of the input voltage sensing circuit is scaled to the PFC input level which presented as the \( V_{\sin(\omega t)} \) in Fig. 6. The \( V_{\text{square}} \) is the output voltage of the comparator, which is produced from the input line voltage. The third harmonic generator, which consists of the PLL and 1/3 counter, also outputs the \( V_{\text{PLL}} \), which has three times the fundamental frequency. Then, the sinusoidal third harmonic, which is presented as the \( V_{\sin(3\omega t)} \), can be obtained by the BPF (band pass filter). Next, the third harmonic injected waveform can be made by adder, which combines \( V_{\sin(\omega t)} \) and \( V_{\sin(3\omega t)} \).

Finally, since the PFC controller needs the rectified voltage for the input, the rectified voltage \( V_{\text{rectifier}} \) of \( V_{\sin(\omega t)} + V_{\sin(3\omega t)} \) is obtained. Additionally, since a BPF must have the correct center frequency with a narrow bandwidth, an inductor of the BPF is replaced with the GIC (generalized impedance converter) circuit, which consists
of op-amps, resistors, and a capacitor.

The scheme of the proposed third harmonic injection circuit with PFC is presented in Fig. 9. The proposed circuit can generate a third harmonic that accurately synchronizes to the input line voltage. This makes it easy to control the third harmonic injection ratio because it can be separated from third harmonic generator and input line sensing voltage. The injected third harmonic voltage is first applied to the PFC controller. Then, the input current becomes distorted along the injected voltage. Finally, the capacitance is reduced for the storage capacitor.

Comparing to conventional circuits as shown Fig. 5, the proposed circuit can control the third harmonic ratio, and it has faster response time because of fast settling time of the PLL and the pure third harmonic can be injected without generating other harmonics. Moreover if the proposed circuit is realized with the PFC IC, the circuit could be simpler and its cost could be lower.

4. Experimental Verification

A prototype of boost type PFC (80W) was implemented to validate the proposed third harmonic injection circuit. The Wave Runner 104MXi Oscilloscope (LeCroy) and the WT 500 Power Analyzer (YOKOGAWA) were used for measurement. Specifications and design parameters are as follows:

(1) Input voltage: 220(198~242)Vac/60Hz
(2) Output voltage: 400Vdc
(3) Output power: 80W
(4) Input filter capacitor: 100nF
(5) Input filter inductor: 50mH
(6) Switch: 6N80C (Fairchild)
(7) Diode: US3M
(8) Boost inductor: 1.3mH
(9) Controller: MC33262 (On a semiconductor)
(10) PLL IC: 74HC4046 (On a semiconductor)
(11) Op-amp: TL084 (ST)

The generated third harmonic waveform and waveforms of the PLL input/output are presented in Fig. 10.

![Fig. 9. Schematic of third harmonic injection circuit and PFC](image)

![Fig. 10. Waveforms for third harmonic generation](image)

As shown in Fig. 9, the square waveform generated by the PLL is three times the fundamental frequency of \( V_{\text{square}} \) which is sensed from the input line voltage by a sensing circuit. A generated signal can be synchronized to input voltage and changed to the function of sinusoidal, which is the third harmonic of the BPF using the GIC. A red line is \( V_{\text{square}} \), a yellow line is \( V_{\text{PLL}} \), and blue line is \( V_{\text{sin}(3\omega t)} \). Since the fundamental frequency is 60Hz, the frequency of the third harmonic is 180Hz.

The third harmonic injection signal is summed with the generated third harmonic signal and the sensed input line voltage. The output of a summing circuit, which is a third harmonic injection signal, is injected to the PFC controller.

Fig. 11 shows the input current, input voltage, and output DC voltage of the PFC when the third harmonic injection circuit is applied. The yellow line is the DC link voltage \( V_c(t) \), which is the output of the PFC; the red line is the input current \( I_L(t) \); the blue line is the input voltage \( V_{\text{in}}(t) \); and the green line is a input pin of the PFC controller \( V_{\text{rectifier}}(t) \), when the third harmonic is injected into the input current.

![Fig. 11. Waveforms for third harmonic injections](image)
Fig. 12. Waveform of variation of THD for third harmonic current injection ratio of (a) 8%, (b) 12% (c) 16%, (d) 20%, (e) 24%, (f) 28%

Fig. 13. PF variation by third harmonic injection ratio

Fig. 14. IEC 61000 and THD variation according to the third harmonic injection ratio
installed film capacitor of 6.8uF instead of 8.8uF. The ripple voltage $\Delta V_C$ of the output DC voltage was measured as 77V$_{p-p}$ which is the same value as the THD 8% when the capacitance of the PFC is 8.8uF. The dynamic range of input voltage with the implemented PFC is from 198v to 244v and the frequency range is from 50Hz to 60Hz.

5. Conclusion

This paper proposed using a new third harmonic injection circuit with a single stage PFC to reduce storage capacitance. As a result, the lifetime of LED lighting can be extended by replacing the electrolytic capacitor with the film capacitor.

The conventional circuits for replacing the electrolytic capacitor with film capacitor are hard to control the third harmonic ratio. Therefore, existing methods are hard to satisfy the required power factor and THD of various environments. Furthermore, these circuits easy to produce the unwanted harmonics. However, the proposed circuit for third harmonic injection can generate the pure third harmonic and control it easily.

The proposed circuit consisted of a PLL, a 1/3 counter, and op-amps to generate a third harmonic input current, which were applied to a prototype 80WPFC circuit. The reduced storage capacitance was verified experimentally by increasing the third harmonic injection ratio of the input current.

However, LED drivers have a THD limit of IEC 61000 Class C. Consequently, the third harmonic injection ratio has to be 28% to satisfy the THD limit. The determined ratio can achieve a 75% reduction of the storage capacitance. The proposed circuit has a simple control method and circuitry compared with conventional circuits.

Experimental results showed that the proposed circuit can reduce the storage capacitance value to eliminate the electrolytic capacitor.

Acknowledgements

This research was supported by the MKE(The Ministry of Knowledge Economy), Korea, under the Convergence-ITRC(Convergence Information Technology Research Center) support program (NIPA-2012-C6150-1101-0002) supervised by the NIPA(National IT Industry Promotion Agency)

References


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