A Novel Circuit for Characteristics Measurement of SiC Transistors

Guoen Cao* and Hee-Jun Kim†

Abstract – This paper proposes a novel test circuit for SiC transistors. On-state resistance under practical application conditions is an important characteristic for the device reliability and conduction efficiency of SiC transistors. In order to measure the on-state resistance in practical applications, high voltage is needed, and high current is also necessary to ignite performance for the devices. A soft-switching circuit based on synchronous buck topology is developed in this paper. To provide high-voltage and high-current stresses for the devices without additional spikes and oscillations, a resonant circuit has been introduced. Using the novel circuit technology, soft-switching can be successfully realized for all the switches. Furthermore, in order to achieve accurate measurement of on-state resistance under switching operations, an active clamp circuit is employed. Operation principle and design analysis of the circuit are discussed. The dynamic measurement method is illustrated in detail. Simulation and experiments were carried out to verify the feasibility of the circuit. A special test circuit has been developed and built. Experimental results confirm that the proposed circuit gives a good insight of the devices performance in real applications.

Keywords: SiC, On-state resistance, Test circuit, Measurement

1. Introduction

Silicon-carbide (SiC) transistors are gaining popularity for their enormous potential [1-4]. Recent demonstrations show that SiC transistors can attain outstanding properties such as higher electron density, lower drain-to-source on-resistance, lower thermal resistance, and higher breakdown voltage in comparison to silicon (Si) counterparts [5-10]. Although much progress has been achieved in the development of new power devices, power converters that employ SiC transistors have not become commercially available, because device performance issues under switching operation have not been sufficiently discussed yet [11-14].

To improve these promising next-generation power devices, it is also highly desirable to evaluate the characteristics, such as on-state resistance, during device measurements, especially under realistic power electronics conditions [15-17].

The traditional method to characterize on-state resistance is the pulse I-V step measurement, which is shown in Fig. 1. This technique requires special equipment and cannot mimic the actual applications. However, few research papers have been produces to measure dynamic on-state resistance of the new devices over the past years [18-20]. In [18] a VIENNA boost converter to character the GaN transistors under operating condition is developed using a Wilson current mirror based circuit to measure dynamic

† Corresponding Author: Dept. of Electronic Systems Engineering, Hanyang University, Korea. (hjkim@hanyang.ac.kr)
* Dept. of Electronic Systems Engineering, Hanyang University, Korea. (caoguoen@hanyang.ac.kr)
Received: December 26, 2013; Accepted: March 1, 2014

Fig. 1. The traditional method to measure on-state resistance.

drain-to-source voltage of the devices. The converter can be used to measure dynamic on-state resistance, gate charge, miller charge, and switching time, etc. But the clamp voltage contains a spike at the transition to the off-state of the switching device. In [20] a voltage clamp circuit using power MOSFET and zener diode is presented. This technique can test GaN transistors in soft-switching and hard-switching conditions. However, the measured dynamic drain-to-source voltage can be influenced by the auxiliary MOSFET body diode and its application is limited.

In addition, to evaluate a power switch under actual switching operation [5, 20, 21], the extreme conditions (e.g., high voltage and high current) should be implemented. Unfortunately, simultaneously high voltage and current power supply (e.g., 400V/50A) in a test laboratory are difficult due to the limited capacity of power installation. Furthermore, reproduction of high voltage and current stresses by means of direct testing should be confronted with huge equipment.

In this paper, a novel and effective measurement technique for SiC transistors has been presented which
involves typical equipment. This proposed technique could reproduce the voltage and current stresses equal to or greater than those which meet in real applications by employing common power supplies. This is one of the merits of the proposed test circuit. To avoid the measurement saturation of oscilloscope, a new and simple voltage clamp circuit is developed with achieving accurate measurement of on-state resistance, which is another merit of the circuit. The proposed circuit gives a good insight of devices performance in real applications. Simulation and experimental results under extreme conditions confirm the validity of the proposed circuit.

This paper is organized as follows. Section II describes the operation principle and detailed analysis of the circuit. Section III discusses the design procedure of the proposed circuit. Section IV explains the measurement method of the on-state resistance, which is another merit of the circuit. The proposed circuit gives a good insight of devices performance in real applications. Simulation and experimental results under extreme conditions confirm the validity of the proposed circuit.

2. Circuit Configuration and Operation

2.1 Circuit configuration

The configuration of the proposed circuit is shown in Fig. 2. The main structure of the circuit is based on a synchronized buck converter which is designed to operate in discontinuous inductor current mode (DCM).

The test system consists of a voltage source $V_{H}$, an upper side Si power MOSFET $Q_{H}$, a current source $V_{L}$, an ultra-fast diode $D$, an LC filter, an active voltage clamp circuit, and DUT (device under test), where $Q_{DUT}$, $D$, $LC$ filter and the DUT compose the basic synchronized buck converter.

In the configuration, $C_{Qaux}$ and $C_{DUT}$ are denoted as the equivalent output capacitances of $Q_{aux}$ and $Q_{DUT}$, respectively, which consist of the drain-to-source and snubber capacitance of each switch. The high side MOSFET, $Q_{H}$, and the DUT operate complementarily with a variable dead-time. The auxiliary Si MOSFET, $Q_{aux}$, operates synchronously with the DUT. The series LC filter together with a damping power resistor $R_{L}$ is connected to the positive terminal of the low voltage high current power supply $V_{L}$ directly.

As the same with conventional synchronized buck converter, the main function of $Q_{H}$ is to provide high voltage stress during the off-state of the DUT. The diode $D$ is used to provide a free-wheeling path for the inductance current $i_{L}$, to impede high voltage stress from $V_{H}$, and the most important, to supply high current stress to the DUT. The main function of the inductor $L$ is to absorb the energy stored in the output capacitance of $Q_{DUT}$, $Q_{aux}$ and $D$ to realize soft switching by resonance during transitions. The capacitor $C_{R}$ is used to store the energy delivered by $L$, and prevent any potential DC voltage from $V_{H}$ to $V_{L}$.

As shown in Fig. 2, $R_{f}$ is denoted as a thermally protected fusing resistor for over-current protection of $V_{H}$. $R_{l}$ is a low value power resistor to limit the current stress of DUT. In the conventional synchronized buck converter, $R_{l}$ is the load of the converter, consuming a lot of power.

The voltage clamp circuit consists of the auxiliary switch $Q_{aux}$ and the blocking capacitor $C_{clamp}$ which are parallel with the DUT. The measurement principle of the circuit will later be illustrated in Section III.

2.2 Circuit operation principles

To understand the voltage and current stresses of the DUT and to analyze the switching characteristic in detail, it is necessary to explain the operation principles of the circuit and some important equations during transitions.

To simplify the analysis, it is assumed that all the switching devices are ideal except the above illustration.
The capacitance of $C_R$ is assumed large enough so that the voltage on it, denoted as $V_{CR}$, stays constant approximately. As the inductor is operated in DCM, the inductance current $i_L$ would change direction before the next switching cycle.

The operation of the circuit can be divided into eight main stages in one switching period. The signal control

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**Fig. 4.** Equivalent circuits for each operation mode: (a) Stage 1 [$t_0 - t_1$]; (b) Stage 2 [$t_1 - t_2$]; (c) Stage 3 [$t_2 - t_3$]; (d) Stage 4 [$t_3 - t_4$]; (e) Stage 5 [$t_4 - t_5$]; (f) Stage 6 [$t_5 - t_6$]; (g) Stage 7 [$t_6 - t_7$]; (h) Stage 8 [$t_7 - t_8$].
sequence of the switches and the corresponding key waveforms of the operation are illustrated in Fig. 3. Fig. 4 shows the conduction path and current direction in every transition. The detailed analysis of this converter will be thoroughly examined in the following.

Stage 1 \([t_0 - t_1]\) [see Fig. 4(a)]: This stage begins at \(t_0\) when the high side switch, \(Q_H\), is in on state and the high voltage is applied to \(L_r\) and \(C_r\). The inductance current \(i_{Lr}\) increases linearly from zero with the ramp rate controlled by \(V_{H}\) and \(L_r\) ending at a peak current value \(i_{t_1}\). The inductance value is designed big enough that \(i_{t_1}\) increases slowly with a very small average value. The DUT and \(Q_{aux}\) are in off state so that high voltage stress is applied to DUT. The voltage across \(C_{clamp}\) is clamped at a low level value as there is no current circulation through \(Q_{aux}\), which is the main function of the voltage clamp circuit. \(V_{CR}\) is charged up by the inductor current. The inductance current \(i_{t_1}\) and the drain-to-source voltage of DUT \(v_{DS\_DUT}(t)\) are given by

\[
\begin{align*}
  i_{t_1}(t) & \approx \frac{V_H - V_{CR} - V_L}{L} (t - t_0), \\
  v_{DS\_DUT}(t) & = i_{t_1}(t) R_l \approx V_H.
\end{align*}
\]

In this stage, the current stress of the DUT is zero.

Stage 2 \([t_1 - t_2]\) [see Fig. 4(b)]: This stage starts by turning \(Q_H\) off, and thus, \(v_{DS\_H}\) begins to increase. Because of the dead-time between gate driver signals, DUT and \(Q_{aux}\) are still in off state. As shown in Fig. 4(b), \(V_L\) is lower than the voltage across the DUT. The diode current \(i_{Diode}\) cannot flow and \(D\) is reverse biased. A resonance starts among \(L_r\), \(C_{clamp}\) \(C_{aux}\), \(C_{DUT}\), and \(C_{QH}\). Due to the resonant nature, when \(v_{DS\_DUT}\) decreases to \(V_L + V_{CR}\) at time \(t_2\), the inductance current \(i_{Lr}\) reaches to its maximum value \(i_{LMax}\). As a result, \(i_{Lr}\) first increases and then decreases in a very short period. In addition, the DUT current \(i_{DUT}\) continues to flow through its output capacitance \(C_{DUT}\) until \(v_{DS\_DUT}\) is equal to \(V_L\). Along with the decreasing of \(v_{DS\_DUT}\), the clamped voltage \(V_{clamp}\) also decreases. During the interval \([t_1 - t_2]\), \(i_{Lr}\) and \(v_{DS\_DUT}\) are expressed as

\[
\begin{align*}
  i_{t_2}(t) & = i_{t_1}(t) + \frac{V_L}{Z_0} \sin \omega_b (t - t_2), \\
  v_{DS\_DUT}(t) & = v_{DS\_DUT}(t_2) \cos \omega_b (t - t_2).
\end{align*}
\]

where \(i_{LMax}\) is the resonant peak value of \(i_{Lr}\), \(Z_0\) is the equivalent impedance of the resonant circuit, 

\[
\omega_b = \frac{1}{\sqrt{(C_{QH} + C_0) L}},
\]

\[
Z_0 = \frac{L}{\sqrt{(C_{QH} + C_0)}},
\]

As for the interval time \([t_2 - t_3]\), the voltage applied to DUT decreases from \(V_L + V_{CR}\). This stage period \(t_{12}\) is

\[
t_{12} = \frac{\pi}{\omega_b} = \frac{\pi}{\sqrt{(C_{QH} + C_0) L}}.
\]

Stage 3 \([t_2 - t_3]\) [see Fig. 4(c)]: Once \(v_{DS\_DUT}\) reaches \(V_L\) at time \(t_3\), diode \(D\) is forward biased and provides a freewheeling path for the inductance current and the resonance process is stopped. During this stage, the voltage applied to \(Q_H\), \(V_{DS\_H}\) is kept at \(V_L + V_D\). Meanwhile, the energy associated with \(L_r\) is drawn to the “load” resistor \(R_L\). As a result, the inductance current \(i_{Lr}\) decreases at a slow rate. The time of this stage is prescribed by the dead-time control. The voltage stress of \(Q_{DUT}\) is

\[
v_{DS\_DUT}(t) = V_L - V_D,
\]

where \(V_D\) is the forward voltage of the diode \(D\). The current stress of \(Q_{DUT}\) is zero within this period.

Stage 4 \([t_3 - t_4]\) [see Fig. 4(d)]: At time \(t_3\), the DUT and \(Q_{aux}\) are turned on synchronously. Since the voltage \(V_L - V_D\) is much lower than \(V_{H}\), the switches are operated under ZVS approximately. The high current stress supplied by \(V_L\) are applied to the DUT. By proper design of auxiliary circuit and gate driver timing, as discussed in the next section, the clamped voltage applied to \(C_{clamp}\), \(v_{clamp}\), goes closely approximate to \(v_{DS\_DUT}\) in a high precision. Within this period, the inductance current \(i_{Lr}\) continues flowing through the diode and decreasing linearly. The drain-to-source voltage of \(Q_{DUT}\) increases to \(V_L - v_{DS\_DUT}\). At the end of this interval, \(i_{Lr}\) falls down to zero. During this stage, the voltage and current stresses across to DUT can be expressed as:

\[
i_{DS\_DUT}(t) = \frac{V_L - V_D}{R_L + r_{DS\_on}},
\]

and

\[
v_{DS\_DUT}(t) = r_{DS\_on} i_{DS\_DUT}(t),
\]

respectively, where \(r_{DS\_on}\) is the dynamic on resistance of the DUT.

Stage 5 \([t_4 - t_5]\) [see Fig. 4(e)]: At time \(t_4\), the inductance current \(i_{Lr}\) reverse its polarity and starts to increase from zero. As the DUT and \(Q_{aux}\) are still in on state during this period, the diode \(D\) continues conducting with a very low impedance, indicating that the inductance current \(i_{Lr}\) will mainly flow through \(D\) rather than DUT. Therefore, the influence of \(i_{Lr}\) to \(i_{DS\_DUT}\) can be neglected, especially when
\( i_{DS\_DUT} \) is much bigger than \( i_{Lr} \). In this interval, the voltage and current stresses to the DUT are the same with Stage 4. The inductance current \( i_{Lr} \) is given by

\[
i_{Lr}(t) = \frac{V_{ds\_DUT}}{L} (t-t_s).
\]

(12)

Stage 6 \([t_s - t_6]\) [see Fig. 4(f)]: This stage starts by turning the DUT and \( Q_{aux} \) off. Due to the existence of \( C_{Qaux} \) and \( C_{DUT} \), the switches are turned off under ZVS. As there is a dead-time, \( Q_H \) keeps off in this stage. Once DUT is turned off, the diode \( D \) starts the reverse recovery process in a very short interval, after which a resonance occurs among \( L_r, C_{clamp}, C_{Qaux}, C_{DUT}, \) and \( C_{QH} \). Thus, \( C_{clamp}, C_{Qaux} \) and \( C_{DUT} \) are charged while \( C_{QH} \) is discharged. At time \( t_6 \), \( v_{DS\_DUT} \) increases to \( V_{CR} \), and the inductance current \( i_{Lr} \) reaches its maximum value \( i'_{LMax} \) in the opposite direction. Therefore, the inductance current \( i_{Lr} \) first increases and then decreases after a very short period. Meanwhile, as the capacitance \( C_{clamp} \) is much bigger than \( C_{Qaux} \), the clamped voltage \( V_{clamp} \) are kept in a very low level comparing with \( v_{DS\_DUT} \). The voltage stress applied to the DUT equals to the capacitance voltage of \( C_{DUT} \), which is given by

\[
v_{DS\_DUT}(t) = V_H + (V_H - V_S) \sin \omega_b(t).
\]

(13)

As the resonant circuit constitution in this stage is the same with in Stage 2, we can get that \( i_{LMax} = i'_{LMax} \). Comparing with \( V_H \) and \( V_{CR} \), \( V_{CL} \) is significantly small, thus, the parasitic capacitors’ charging time from 0 to \( V_{CL} \) is very short and can be neglected. In addition, since \( i_{Lr} \) is considerable small, current stress of the DUT in this stage can be neglected. This stage period \( t_{66} \) can be expressed as

\[
t_{66} \approx \frac{\pi}{\omega_b} = \pi \sqrt{\frac{C_{QH} + C_Q}{L}}.
\]

(14)

The inductance current \( i_{Lr} \) is given by

\[
i_{Lr}(t) = i'_{LMax} \cos \omega_b(t).
\]

(15)

Stage 7 \([t_6 - t_7]\) [see Fig. 4(g)]: At time \( t_6 \), the voltage of \( C_{DUT} \) is charged up to \( V_{CS} \) and the drain-to-source voltage of \( Q_H \) falls down to zero. Thus, the body diode of \( Q_H \) starts to conduct and provides a freewheeling path to the inductance current \( i_{Lr} \). The resonance process ends at \( t_7 \), and therefore, \( i_{Lr} \) decreases linearly with a small average value

\[
i_{Lr}(t) = i_L(t_6) - \frac{V_H - V_{CR} - V_{CL}}{L} (t-t_6).
\]

(16)

As a result, during this period, the voltage stress of the DUT is given by

\[
v_{DS\_DUT}(t) = V_H + i_L(t)R_L,
\]

(17)

and the current stress is zero. In addition, the clamped voltage \( v_{clamp} \) is kept at its maximum value.

Stage 8 \([t_7 - t_8]\) [see Fig. 4(h)]: \( Q_H \) is turned on at time \( t_7 \). Since the body diode is in on state, the switch is operated under ZVS. The high voltage stress \( V_{H}+i_L(t)R_L \) is still applied to the DUT and the voltage clamp circuit. The freewheeling path of the inductance current \( i_{Lr} \) changes to \( Q_H \) from the body diode.

This stage ends when the inductance current \( i_{Lr} \) reaches zero and begins to increase in the opposite direction. Therefore, at the moment \( t=t_8 \), one switching cycle is completed and a new switching cycle starts.

3. Analysis of the Measuring Stage

In order to improve the reliability and performance of new power devices, the characteristics measurement should be discussed under practical operations. From the principle analysis in the previous section, the proposed circuit can represent real operating circumstances, and gives a good insight into the performance of the devices in practical applications. The proposed system, which is a combination of a regular synchronous buck topology, a low voltage high current power supply, and an active clamp circuit comprising an additional switch and a capacitor, makes it possible to measure various characteristics under real power applications, such as high voltage and high current conditions.

The main circuit can be designed like a regular synchronized buck converter which works in DCM. However, unlike the conventional synchronous buck converter, the main concept of the proposed system is to perform the characteristics measurement of SiC transistors. Therefore, the design considerations have a lot of differences, which are important during measurements, such as operation mode, power capacity, and dead-time of control signals.

To achieve ZVS of the DUT, it is necessary that the energy stored in \( L_r \) at the moment \( Q_H \) turning off should be larger than or equal to the energy required to discharge the output capacitance of \( Q_H, Q_{aux} \) and \( Q_{DUT} \) down to zero.

Furthermore, reduction of the peak voltage and current stresses of the DUT can be achieved by adjusting the inductance current and the dead-time of driving signals. The dead-time is needed to avoid cross conduction between the switches and to realize soft-switching.

From the analysis in Section II, the ZVS conditions can be expressed as:

\[
v_{DS\_DUT}(t_s) \leq V_L,
\]

(18)

and

\[
v_{DS\_DUT}(t_s) \geq V_H.
\]

(19)
Therefore, we have

\[ V_H - (V_{CR} + V_L) \geq V_{CR}, \]  

(21)

and

\[ t_{\text{deadtime}} \geq t_{\text{on}} \approx t_{\text{on}}. \]  

(22)

During the dead-time the voltage over DUT cannot decrease below input voltage \( V_L \). Therefore, the maximum reasonable dead-time is the one that is needed to lower the voltage over the switch to \( V_L \) level. A longer dead-time would be unnecessary. A certain amount of magnetizing current is required in order to reduce the voltage level over the DUT switch prior to its turn-on.

Based on the superposition theorem and boundary conditions of operation mode of the converter, when operating in critical conduction mode (CrM), we can get that

\[ V_{CR} \approx (V_H + V_H)D, \]  

(23)

where \( D \) is the duty ratio of the CrM converter.

From (21) and (23), the ZVS conditions (18) and (19) can be simplified as:

\[ D \leq 0.5 \]  

(24)

From the conventional critical inductance design, the maximum value of \( L \) can be designed as:

\[ L_{\text{max}} = \frac{V_{CR} \left(1 - \frac{V_{CR}}{V_H}\right)}{2f_s i_{\text{on}}} \]  

(25)

where \( f_s \) is the switching frequency.

In actual applications, waveforms contain spikes and oscillations. In this proposed circuit, it is possible to turn on the main switch at a relatively low voltage level with the help of the series \( LC \) filter, and therefore, the influence of peak voltage stress can be reduced.

The electrical performance of the device represents its viability in power applications. SiC transistors are still in a development stage, therefore, there is a good opportunity to study, design, and test not only a device but also the processes involved. This test circuit provides a very helpful tool to get an optimal design.

**4. Dynamic On-resistance Measurement Method**

The measurement method of DUT dynamic on-resistance operating in switching mode is based on the Ohms law, being calculated by dividing \( V_{DS\text{on}} \) by \( i_{DS} \)

\[ r_{DS\text{on}}(t) = \frac{V_{DS\text{on}}(t)}{i_{DS}(t)} \]  

(26)

In real applications, the drain-to-source voltage of the DUT usually swings in a large range such as hundreds of volts in the off-state and several millivolts in the on-state. Direct measurement using oscilloscope voltage probes either gives poor accuracy or causes saturation of the oscilloscope channel. To avoid these problems, an active clamp circuit is employed in the proposed system to avoid the oscilloscope saturation in off-state.

Fig. 5 presents the equivalent configuration of the active clamp circuit. The operation principle is discussed in Section II and shown in Fig. 3. The output voltage waveform \( V_{DS}(t) \) of the DUT is measured between the nodes A and B using a differential probe. \( R_{\text{probe}} \) denotes the impedance of the oscilloscope probe, which is about \( 1 \text{M}\Omega \) generally. \( r_{Q_{\text{aux}}} \) and \( r_{DS\text{on}} \) denote the on-state resistance of \( Q_{\text{aux}} \) and DUT, respectively.

As shown in Fig. 5(a), when DUT and \( Q_{\text{aux}} \) are turned off, high voltage stress \( V_{DS\text{off}} \) is applied to the DUT and the active clamp circuit. The measured value of the probe can be expressed as follows:

\[ V_{\text{clamp off}} = \frac{V_{DS\text{off}} R_{\text{probe}} Z_{\text{clamp}}}{R_{\text{probe}} Z_{\text{clamp}} + Z_{\text{Q_{aux}}}} \]  

(27)

**Fig. 5.** Equivalent circuits for measurement: (a) off state; (b) on state.
where \( Z_{\text{clamp}} \) and \( Z_{\text{Qaux}} \) are the equivalent impedance of \( C_{\text{clamp}} \) and \( C_{\text{Qaux}} \), respectively. In the system design, it is easy to achieved that

\[
R_{\text{probe}} \gg Z_{\text{clamp}}, \quad Z_{\text{Qaux}} \gg Z_{\text{clamp}}. \tag{28}
\]

Therefore, the measured voltage \( v_{\text{clampoff}} \) can be clamped and approximated as

\[
v_{\text{clampoff}} = V_{\text{DSoff}} \cdot \frac{Z_{\text{clamp}}}{Z_{\text{Qaux}}}, \tag{29}
\]

indicating that the measured result is “clamped” at a considerable small value comparing with \( V_{\text{DSoff}} \).

During the on-state of the DUT, as shown in Fig. 5(b), a high current stress is applied to the DUT along with a very small drain-to-source voltage. The measured voltage across \( C_{\text{clamp}} \) can be calculated by

\[
v_{\text{clampon}} = \frac{V_{\text{DSon}}}{R_{\text{probe}} Z_{\text{clamp}} + r_{\text{Qaux}} (R_{\text{probe}} + Z_{\text{clamp}})}, \tag{30}
\]

where \( r_{\text{Qaux}} \) is very small with only tens of milli-ohm generally. As \( Z_{\text{clamp}} \gg r_{\text{Qaux}} \), the measured \( v_{\text{clampon}} \) can be simplified as

\[
v_{\text{clampon}} = \frac{V_{\text{DSon}}}{R_{\text{probe}} Z_{\text{clamp}}} = V_{\text{DSon}}, \tag{31}
\]

which means the measured voltage is extremely close to the real value \( V_{\text{DSon}} \).

Assuming that \( r_{\text{DSon}} \) of the DUT and \( Q_{\text{H}} \) are 90mΩ and 45mΩ, respectively, the output capacitances of \( Q_{\text{aux}} \) and the DUT are 500pF, \( C_{\text{clamp}} \) is 0.1µF, the switching frequency is 50 kHz, and the on-state DUT current is 1A. We can get that during off state,

\[
v_{\text{clampoff}} = 400 \times \frac{0.5}{0.1 \times 10^5} V = 2V, \tag{32}
\]

while during on state

\[
v_{\text{clampon}} = \frac{0.09 \times 1 \times 10^{-6}}{0.1 \times 10^{-6} + 0.045 (1 \times 10^{-6} + \frac{1}{0.1 \times 10^{-6}})} \approx 0.09V = V_{\text{DSon}}. \tag{33}
\]

According to the example result, the active clamp circuit can measure the on-state \( V_{\text{DSon}} \) dynamically without the influence of high voltage swing. The value of the off-state clamped voltage \( V_{\text{clampoff}} \) can be adjusted by using different clamp capacitors. Based on (26), the dynamic on-state resistance of the DUT can be calculated with a high precision.

5. Simulation and Experimental Results

5.1 Simulation results

Based on the operation analysis, a PSIM model of the proposed system has been developed. A comprehensive simulation was conducted to verify the performance of the test circuit.

In order to examine the proper performance of the rectifier in practical applications, actual semiconductor models of the power devices were employed.

The experimental waveforms are shown in Figs. 6 and Fig. 7. The driver signals, drain-to-source voltages of DUT and \( Q_{\text{H}} \), and the current waveforms of DUT and \( L_r \) are shown in Fig. 6. According to the waveforms, soft-

![Fig. 6. Simulation switching results.](image)

![Fig. 7. Simulation results of the on-state resistance measurement circuit.](image)
switching is achieved for both of the DUT and $Q_H$. It can be observed that the inductance current is small enough that the influence on the DUT current can be insignificant.

The simulation waveforms of the voltage clamp circuit are shown in Fig. 7. While the drain-to-source voltage $V_{ds}$, DUT swings between on-state voltages to up to 400V, the clamped voltage $V_{clamp}$ changes from on-state voltage to around 2.5V. The clamped on-state voltage is 0.770143V which is very close with the real voltage 0.770427V. Therefore, using the voltage clamp circuit, on-state resistance can be circulated in a high precision.

5.2 Experimental results

A prototype of 400V/10A capacity circuit was performed to verify the theoretical analysis of the proposed circuit. The photograph related to the experimental circuit is given in Fig. 8. Some parameters of the prototype circuit are listed in Table 1. A SiC transistor manufactured by ROHM, SCH2090KE, is chosen as the DUT. The key parameters of the device are shown in Table 2 with reference to the device datasheet. To avoid the temperature influence, a big heatsink and two high power fans were employed during experiments, making sure that the device temperature was kept in 28°C ~ 30°C.

Experiments have been carried out to verify the analysis. The switching waveforms of DUT and $Q_H$ are shown in Figs. 9 and Fig. 10. In Fig. 9, the voltage, current, and control waveforms of the DUT are illustrated. As the same with simulation results, the switches DUT and $Q_H$ are operated under soft-switching at both turn-on and turn-off.

It should be noted that there is no overlap and oscillation in voltage and current waveforms. In addition, from the waveforms it can be seen that during the off state of the DUT, the device voltage stress can reach up to 400V, while during the on state, the device current stress is up to 10A. Comparing with the DUT current, the inductance current is small enough, and thus, the power loss consumed by $R_L$ can also be very small.

The measured waveforms of active clamp circuit are given in Fig. 11. To measure the on-state voltage and

### Table 1. Parameters of the prototype circuit

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>High voltage source</td>
<td>$V_H$</td>
<td>0–400VDC</td>
</tr>
<tr>
<td>Low voltage source</td>
<td>$V_L$</td>
<td>0–50VDC</td>
</tr>
<tr>
<td>High current range</td>
<td>$I_D$</td>
<td>0–50A</td>
</tr>
<tr>
<td>High side switch</td>
<td>$Q_H$</td>
<td>IPW60R045CP</td>
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<td>Auxiliary switch</td>
<td>$Q_{aux}$</td>
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</tr>
<tr>
<td>DUT</td>
<td>$Q_DUT$</td>
<td>SCH2090KE</td>
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<tr>
<td>Resonant inductance</td>
<td>$L_r$</td>
<td>600µH</td>
</tr>
<tr>
<td>Output capacitor</td>
<td>$C_R$</td>
<td>200µF</td>
</tr>
<tr>
<td>Clamp capacitor</td>
<td>$C_{clamp}$</td>
<td>1µF</td>
</tr>
<tr>
<td>“Load” resistance</td>
<td>$R_L$</td>
<td>1kΩ</td>
</tr>
</tbody>
</table>

### Table 2. Parameters of DUT in the prototype circuit

<table>
<thead>
<tr>
<th>Items</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device type</td>
<td>N channel SiC MOSFET</td>
</tr>
<tr>
<td>Device package</td>
<td>TO-247</td>
</tr>
<tr>
<td>Drain-source breakdown voltage</td>
<td>1200V</td>
</tr>
<tr>
<td>Drain-source maximum current</td>
<td>26A</td>
</tr>
<tr>
<td>On-state resistance ($V_{gs} = 18V$)</td>
<td>90mΩ</td>
</tr>
<tr>
<td>Total gate charge ($V_{gs} = 18V$)</td>
<td>98µC</td>
</tr>
</tbody>
</table>

Fig. 8. The prototype of the proposed test circuit.

Fig. 9. Experimental switching waveforms of the proposed circuit. $V_{GS}$: driver signal of DUT, $V_{DS}$: drain-to-source voltage of DUT, $V_{DS,HS}$: drain-to-source voltage of $Q_H$, $I_{DS}$: drain-to-source current of DUT.

Fig. 10. Experimental waveforms of the proposed circuit. $V_{GS}$: driver signal of DUT, $V_{DS}$: drain-to-source voltage of DUT, $V_C$: voltage across $C_R$, $I_L$: inductance current.
current accurately and steadily, the switching frequency was set at 50 kHz. And to eliminate the device temperature increasing, the maximum drain-to-source current was set at 6A. According to the waveforms, the auxiliary switch $Q_{aux}$ was activated synchronously with the DUT. During off state of the switches, the clamped voltage $V_{clamp}$ was clamped at lower than 3V, while the actual drain-to-source voltage of the DUT was up to 400 V. During the on state, $V_{clamp}$ can indicate the real value of the DUT voltage.

These results were quite similar to those in the previous study where switching waveforms were simulated.

Figs. 12 to Fig. 17 described the experimental results on the $r_{DSon}$ measurement using oscilloscope probe directly and the active clamp circuit. To evaluate the on-state performance of the DUT under different conditions, the gate driver voltages of the DUT were set as 10V, 14V, and 18V, respectively. The voltage range for comparison was set as 0 ~ 100V in the experiments. Because of the measurement resolution problems, the on-state resistance could not be measured in a high accuracy for conventional circuits. Especially, as the drain-to-source voltage increases, the oscilloscope should be set from 0.1V/div to 10V/div. As on-state resistance is usually less than 1Ω, direct oscilloscope measurement leads a big problem of measurement error.

Fig. 12, Figs. 14, and Fig. 16 compared the measured results through oscilloscope probe and the active clamp circuit. It can be observed that as the drain-to-source voltage increased, the $r_{DSon}$ which was calculated based on using the probe directly drifted significantly. However, the experimental results via the active clamp circuit kept stable with a high resolution. The measurement errors of the oscilloscope probes were up to 30%, 94%, and 150% under 10V, 14V, and 18V driving voltages, respectively, comparing with the active clamp circuit.

The experimental results under full voltage range of 0 ~ 400V based on the active clamp circuit are shown in Fig. 13, Figs. 15, and Fig. 17. It is shown that under 10V gate voltage, the on-state resistance of DUT varies a little from 0.419Ω to 0.436Ω, while under 14V gate voltage, the resistance varies from 0.1462Ω to 0.1518Ω. Comparing with the value in datasheet, 0.09Ω under 18V gate voltage, the on-state resistance changes from 0.0942Ω to 0.0979Ω.

Fig. 11. Experimental waveforms of active clamped circuit with $V_{GS}=18V$. $V_{DS}$: drain-to-source voltage of DUT, $V_{clamp}$: clamped voltage across $C_{aux}$, $I_{DS}$: drain-to-source current of DUT.

Fig. 12. The comparison results of on-state resistance with $V_{GS}=10V$.

Fig. 13. The experimental result measured by the clamp circuit under full range with $V_{GS}=10V$.

Fig. 14. The comparison results of on-state resistance with $V_{GS}=14V$. 

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According to the results above, the calculated results are almost identical to those simulated and measured. As a result, it can be clearly seen that the predicted theoretical analysis and operation principles of the proposed circuit are experimentally verified.

6. Conclusion

In this study, a novel circuit for SiC transistors characterization measurement has been analyzed in detail. The proposed circuit is based on the conventional synchronous buck converter operating in DCM. By employing two separated normal power supplies, the test system can mimic practical application conditions to test the reliability and performance of the DUT. To overcome the resolution problems when measuring on-state resistance under realistic switching operation, an active clamp circuit is developed. It is observed that the operation principles and the theoretical analysis of the novel circuit are exactly verified by experimental results. It should be noted that the proposed method of this paper could be extended to Gallium Nitride (GaN) devices for current collapse characteristics measurement.

Acknowledgements

This work was supported by the Energy Efficiency & Resources of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) grant funded by the Korea government Ministry of Knowledge Economy. (No. 2012T100100651)

References

A Novel Circuit for Characteristics Measurement of SiC Transistors


Guoen Cao received the B.S degree in electrical engineering from Shandong University of science and technology, Qingdao, China, in 2009 and the M.S. degree in electrical engineering from Beihang University, Beijing, China in 2012. He is currently working toward the Ph.D. degree in electrical engineering with Hanyang University, Ansan, Korea. His research interests are DC / DC converters and soft switching techniques.

Hee-Jun Kim received the B.S and M.S. degree in electronics engineering from Hanyang University, Seoul, Korea, in 1976 and 1978, respectively, and the Ph.D. degree in electronics engineering from Kyushu University, Fukuoka, Japan, in 1986. Since 1987, he has been with the department of Electronic Systems Engineering, Hanyang University, Ansan, Korea, where he is currently a professor. His current interests include switching power converters, electronic ballasts, soft switching techniques, and analog signal processing. Dr. Kim is the president-elect of the Korean Institute of Electrical Engineers (KIEE) and a senior member of IEEE.