A CMOS Bandgap Reference Voltage Generator for a CMOS Active Pixel Sensor Imager

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This paper proposes a new bandgap reference (BGR) circuit which takes advantage of a cascode current mirror biasing to reduce the $V_{\text{ref}}$ variation, and sizing technique, which utilizes two related ratio numbers $k$ and $N$, to reduce the PNP BJT area. The proposed BGR is designed and fabricated on a test chip with a goal to provide a reference voltage to the 10 bit A/D (4-4-4 pipeline architecture) converter of the CMOS Active Pixel Sensor (APS) imager to be used in X-ray imaging. The basic temperature variation effect on $V_{\text{ref}}$ of the BGR has a maximum delta of 6 mV over the temperature range of 25 °C to 70 °C. To verify that the proposed BGR has radiation hardness for the X-ray imaging application, total ionization dose (TID) effect under Co-60 exposure conditions has been evaluated. The measured $V_{\text{ref}}$ variation under the radiation condition has a maximum delta of 33 mV over the range of 0 krad to 100 krad. For the given voltage, temperature, and radiation, the BGR has been satisfied well within the requirement of the target 10 bit A/D converter.

\textit{Keywords}: Bandgap reference(BGR), CMOS APS imager, Cascode current mirror, Total ionization dose(TID)

1. INTRODUCTION

The bandgap reference (BGR) circuit is one of the most popular reference voltage generators used in high precision comparators, A/D or D/A converters, and many other analog circuits to support a stable reference voltage and/or current. So the BGR is required to have good immunity against any supply voltage fluctuations or temperature variations. In addition, to be incorporated into a specific CMOS Active Pixel Sensor (APS) imager targeting an application field of X-ray imaging, the immunity of the BGR under radiation environment is also important.

Related to the BGR, several unique solutions have been suggested\textsuperscript{[1-3]} and their experiment results under severe radiation condition have also been reported\textsuperscript{[4]}. In this paper, another circuit solution is proposed and the test results of voltage characteristic, temperature characteristic, and radiation response of the proposed BGR, targeting a digital X-ray imaging application, are reported. The main focus of this paper is to evaluate the performance of the newly proposed BGR under voltage, temperature variation, and radiation condition, but not to analyze the evaluation results theoretically. For the evaluation, the proposed BGR is actually designed and fabricated on a test chip. To set the design target, the following assumptions were made: The BGR will supply voltage of 2.5 V ±10 % for the A/D converter of a 10 bit A/D (4-4-4 pipeline architecture) which will be embedded in a CMOS APS imager for X-ray imaging.

2. PROPOSED BGR CIRCUIT

The proposed BGR shown in Fig. 1 consists of a differential op-amp, a bias circuit, a cascode current mirror, a level shifter, PMOS transistors with optimally controlled sizes, two PNP bipolar transistors, and resistors.
The cascode current mirror, which has wide swing characteristic and immunity against threshold variation, is used to reduce the variation of \( V_{\text{ref}} \) and temperature (PVT). The level shifter allows the proposed BGR to be fabricated under the processes providing only normal threshold voltage for MOS transistor. If low-\( V_{\text{TH}} \) MOS were to be available, this level shifter may be removed. The optimally controlled size of the PMOS transistors and its merits are discussed in detail below.

The ratio relationship between various components in the circuit is as follows: \( R_3 = kR_1 \), \( MP1a = MP1b = MP3a = MP3b = kWp \) and \( MP2a = MP2b = Wp \). And the voltages \( V_u \) and \( V_v \) are controlled to be the same level by the operation of the level shifter and the differential op-amp. The current \( I_1 \) is \( I_1 + I_2 \), where \( I_1 \) and \( I_2 \) satisfy the following equations,

\[
I_1 = \frac{\Delta V_{BE}}{R_3}, \quad I_2 = \frac{V_{BE1}}{R_3}
\]

where \( \Delta V_{BE} \) is the voltage difference between the two BJTs \( Q_1 \) and \( Q_2 \), and is expressed as,

\[
\Delta V_{BE} = V_{BE1} - V_{BE2} = V_f \ln(kN)
\]

Fig. 1. Diagram of the proposed BGR circuit.

In equation (2), \( V_f \), \( k \) and \( N \) are the thermal voltage, the number of PMOS transistors, and the area of BJT emitter.

Here, the current \( I_1 \) is mirrored to \( I_2 \) and therefore, the output voltage of the proposed BGR, \( V_{\text{ref}} \), becomes

\[
V_{\text{ref}} = kIR_4 = \frac{V_{\Delta BE}}{R_1} + \frac{V_f k \ln(kN)}{R_2}
\]

If \( k \) is chosen to be 2 and appropriate resistance values are used, \( N \) is calculated to be 5. Compared to other BGRs[1,2] of which the value of \( N \) is 100, the proposed BGR needs only 1/20 of the area for the PNP BJT. Depending on the selection of the \( k \) value, \( N \) can be varied to satisfy the needs.

Generally a BGR generates a voltage which is independent of temperature by summing two voltages where one is proportional to absolute temperature (PTAT) and the other is complementary to absolute temperature (CTAT). In the proposed BGR, the PTAT is the voltage difference between two BJTs, \( Q_1 \) and \( Q_2 \), and the CTAT is \( V_{BE1} \). The BGR circuit does not operate properly if \( V_{\text{BIASU}} \) and \( V_{\text{BIASL}} \) follow the \( V_{\text{DD}} \) voltage because the bias current would become zero. This situation may happen during power-up by capacitive coupling between these nodes and \( V_{\text{DD}} \).

That is the reason a start-up circuit is needed for the proposed BGR as shown in Fig. 2. During power-up, if \( V_{\text{BIASU}} \) of the circuit is larger than \( (V_{\text{DD}} - IV_{\text{TH}}) \), the PMOS transistor, MP1, is OFF and the NMOS transistor, MN1, becomes ON as the gate voltage of the MN1 is raised along with \( V_{\text{DD}} \). Once the MN1 is turned on, the \( V_{\text{BIASU}} \) is discharged to ground. The \( V_{\text{BIASL}} \) acts similarly and the \( V_{\text{BIASU}} \) and the \( V_{\text{BIASL}} \) of the BGR guarantees proper bias operation.

Fig. 2. Start-up circuit for the proposed BGR.

3. EVALUATION RESULTS

3.1 Test chip and \( V_{\text{ref}} \) distribution

The proposed BGR is fabricated using the Hynix 0.18 \( \mu m \) triple-well CMOS logic process that provides only normal \( V_{\text{TH}} \) transistor. Fig. 3 shows the photograph of the proposed BGR test chip.

The distribution of the measured \( V_{\text{ref}} \) with 120 samples is shown in Fig. 4. The measurement is taken at the \( V_{\text{DD}} \) of 2.5 V and room temperature. The average \( V_{\text{ref}} \) was 759 mV with \( \sigma = 25.4 \) mV. The use of a resistive material with narrow width accounts for the wide distribution, since a narrower design is more affected by the process variation.
3.2 Voltage and temperature characteristics

The voltage and temperature characteristics of the proposed BGR were evaluated by both simulation and measurement as shown in Fig. 5. And the results were all summarized in Table 1. and 2.

Through the simulation as shown in Table 1, the conventional BGR used single current mirror shows the $V_{\text{ref (max)}}$ variation of 0.5 V, but 0.09 V in the proposed BGR.

This is because that the cascode current mirror supplies a stable current having no concern with the variation of the output voltage in case of increasing the output resistance of the current source. The recommended current sources to increase the output resistance of the current source are the Wilson mirror and the regulated cascode current mirror in addition to the cascode current mirror[5].

The measured temperature characteristic shows that the BGR starts operating at around 1.0 V, the temperature coefficient of the BGR is 0.2 mV/°C, and the operating current is sub-10 µA.

The maximum $V_{\text{ref}}$ from the test result is 6 mV, which is much greater than 0.17 mV from the simulation. This is due to the fact that the temperature coefficients of the JTs and the resistors of the fabricated test chip are slightly different than those of the model parameters used in simulation.

The starting point seems to vary about 0.3 V over the specified temperature range, which is not captured in the simulation result. This may be due to the unstable operation of the start-up circuit within that voltage range. But since that range is far below to target operation voltage range, this phenomenon should be of no problem.

![Fig. 3. Photograph of the test chip.](image)

![Fig. 4. Measured distributions of $V_{\text{ref}}$ for 120 samples at the $V_{\text{DD}}$ (2.5 V) and the temperature (25 °C).](image)

![Fig. 5. Simulation and test results under voltage and temperature variations.](image)

<table>
<thead>
<tr>
<th>$V_{\text{DD}}$</th>
<th>$V_{\text{ref}}$ (max)</th>
<th>Simulation</th>
<th>Test (Proposed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0V</td>
<td>0.5</td>
<td>0.09</td>
<td>3</td>
</tr>
<tr>
<td>2.5V</td>
<td>0.5</td>
<td>0.09</td>
<td>3</td>
</tr>
<tr>
<td>3.0V</td>
<td>0.5</td>
<td>0.09</td>
<td>3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Temp.</th>
<th>$V_{\text{ref}}$ (max)</th>
<th>Simulation</th>
<th>Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 °C</td>
<td>0.17</td>
<td>750.67</td>
<td>757</td>
</tr>
<tr>
<td>45 °C</td>
<td>0.17</td>
<td>750.67</td>
<td>757</td>
</tr>
<tr>
<td>70 °C</td>
<td>0.17</td>
<td>750.67</td>
<td>757</td>
</tr>
</tbody>
</table>
3.3 Radiation responses of the BGR

The radiation response is evaluated by using Co-60 gamma source in KAERI experiment setup. The source to wafer distance was 16 cm and the dose rate was 5 krad/hr. The $V_{\text{ref}}$ at each cumulated dose was measured using HP4155A-semiconductor parameter analyzer in the probe station at the $V_{\text{DD}}$ of 2.5 V and room temperature. Test result is shown in Fig. 6 and is summarized in Table 3. Compared to the results of the voltage and temperature characteristics, the radiation response of the $V_{\text{ref}}$ was relatively more severe.

![Graph showing radiation response](image)

Fig. 6. Test result of radiation response at each cumulated dose.

<table>
<thead>
<tr>
<th>Dose</th>
<th>$V_{\text{ref}}$ (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 krad</td>
<td>751</td>
</tr>
<tr>
<td>50 krad</td>
<td>779</td>
</tr>
<tr>
<td>100 krad</td>
<td>784</td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
</tbody>
</table>

Table 3. Radiation responses of the BGR (Unit: mV).

Basically, the total ionization dose (TID) effect is the main reason for the radiation response of the BGR, since one of the cumulative effects in semiconductor devices for gamma irradiation is due to the charge trapping in the oxide layer[6].

In MOS devices, the TID effect induces mobility degradation, threshold voltage shift, and leakage current increase. Also in the BJT devices, the TID effect induces mobility degradation and leakage current increase, resulting in degradation of the gain. Therefore, the electrical characteristics of the devices may be the result of the combination of the internal structure and the amount of the TID[7-9].

In the BGR, however, the combination of changed electrical properties of the discrete devices makes it more complicated to understand the $V_{\text{ref}}$ change by the radiation dose. It is expected that the TID effect would shift the DC biasing point in the MOS differential amp. In Fig. 1, there can be a mismatch between the two threshold voltages, $V_{\text{TH1}}$ and $V_{\text{TH2}}$, of the MOS transistors, $T_1$ and $T_2$, if the DC bias point is shifted by the increase of radiation dose, which would result in an offset variation. This also has influence on the precision of the cascode current mirror that should be operating in the saturation mode. The mismatch of other electrical parameters such as conductivity, threshold voltage, and gain can also induce current mismatch in the current mirror. In summary, the radiation dose would have heavy influence on the operation of the BGR, resulting in variation of $V_{\text{ref}}$.

4. CONCLUSION

This paper proposes a new BGR circuit which takes advantage of a cascode current mirror biasing to reduce the $V_{\text{ref}}$ variation and a noble sizing technique, which utilizes two related ratio numbers $k$ and $N$, to reduce the PNP BJT area.

The $V_{\text{ref}}$ variation of the BGR has a maximum delta of 6 mV over the temperature range of 25 °C to 70 °C, and 33 mV over the radiation dose range of 0 krad to 100 krad.

Judging from the estimated overall variation over the given voltage, temperature, and radiation range, the proposed BGR can provide an adequate reference voltage to the 10 bit A/D (4-4-4 pipeline architecture) converter of the CMOS APS imager used in the field of X-ray imaging.

Although the $V_{\text{ref}}$ variation of the BGR was relatively more severe than the swing of voltage and temperature, the BGR may guarantee its radiation hardness for its lifetime since the cumulative absorbed dose of 100 krad in X-ray imaging is not general before the failure of other function of the CMOS APS.

REFERENCES


