Random-Oriented $(\text{Bi},\text{La})_4\text{Ti}_3\text{O}_{12}$ Thin Film Deposited by Pulsed-DC Sputtering Method on Ferroelectric Random Access Memory Device

Youn-Ki Lee, Sung-Lim Ryu, and Soon-Yong Kweon[†]

Department of Materials Science & Engineering/ReSEM, Chungju National University, Chungju 380-702, Korea

Seung-Jin Yeom and Hee-Bok Kang

R&D Division, Hynix Semiconductor Inc., Ichon 467-701, Korea

Received August 12, 2011; Revised October 10, 2011; Accepted November 17, 2011

A ferroelectric $(\text{Bi},\text{La})_4\text{Ti}_3\text{O}_{12}$ (BLT) thin film fabricated by the pulsed-DC sputtering method was evaluated on a cell structure to check its compatibility to high density ferroelectric random access memory (FeRAM) devices. The BLT composition in the sputtering target was $\text{Bi}_{4.8}\text{La}_{1.0}\text{Ti}_{3.0}\text{O}_{12}$. Firstly, a BLT film was deposited on a buried Pt/IrO_x/Ir bottom electrode stack with W-plug connected to the transistor in a lower place. Then, the film was finally crystallized at 700°C for 30 seconds in oxygen ambient. The annealed BLT layer was found to have randomly oriented and small ellipsoidal-shaped grains (long direction: ~100 nm, short direction: ~20 nm). The small and uniform-sized grains with random orientations were considered to be suitable for high density FeRAM devices.

Keywords: Ferroelectric capacitor, BLT thin film, Crystallographic orientation, Grain size, Sputtering method

1. INTRODUCTION

Several ferroelectric materials including $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ (PZT) and $(\text{Bi},\text{La})_4\text{Ti}_3\text{O}_{12}$ (BLT) have been extensively studied to evaluate their feasibility as materials of ferroelectric capacitors to be applied in ferroelectric random access memory (FeRAM) [1-4]. The BLT material has many advantages over the PZT material [4-6], such as being fatigue-free on platinum electrodes and having long term reliabilities such as imprint [3,7-9]. In addition, the BLT material having a Bi-layered perovskite structure has strong anisotropy of polarization values [8,10-12]. Therefore, crystallographic orientations in BLT films must be controlled to maximize the polarization value. Uniform grain size must also be obtained to improve the cell-to-cell uniformity of the polariza-

tion value. Recently, we reported that the orientation of the BLT film coated with a metal-organic decomposition (MOD) solution can be controlled by optimization of process conditions [8,13,14]. Extremely narrow window of process conditions gave random-oriented small BLT grains [13,14], which were suitable for high density FeRAM devices. This critical issue of the abnormal grain growth to c-axis was the reason for the evaluation of the physical vapor deposition (PVD) method of the BLT film. In this study, both the microstructure and ferroelectric properties of PVD-BLT films were evaluated in a FeRAM cell structure.

2. EXPERIMENTS

Figure 1 shows the cell structure for a high density FeRAM device [14,15]. The main feature of the novel cell structure, which is called as merged top and plate line (MTP) cell scheme, is that the top-electrode also serves as plate-line and extends in the word-line direction. The key processes of cell structure integration are briefly described in Table 1. A bottom electrode stack of Pt/IrO_x/Ir (100 nm/10 nm/150 nm) was deposited by the sputtering

[†] Author to whom all correspondence should be addressed:
E-mail: sykweon@cjnu.ac.kr

Copyright ©2011 KIEEME. All rights reserved.

This is an open-access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (<http://creativecommons.org/licenses/by-nc/3.0>) which permits unrestricted noncommercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

Fig. 1. Schematic cross-sectional views of merged top and plate line cell structure: (a) bit-line direction, (b) word-line direction, and (c) word-line direction at the end of plate-line.

Table 1. Integration process features of the ferroelectric random access memory device with the novel cell structure of a merged top and plate line.

0.25 mm front-end processes	- Isolation and well formation V_t implantation - Gate formation: WSi_x and poly-Si - Source and drain formation
Double W bit-line	- Interlayer dielectric deposition - Bit-line contact and bit-line formation
Stacked capacitor	- W-plug contact formation - Capacitor formation - Bottom electrode formation (Pt/IrO_x/Ir) - Inter-layer dielectric deposition and SiO_x chemical mechanical polishing (Bi,La)₄Ti₅O₁₂ deposition and rapid thermal annealing process - Top electrode formation
Metallization	- Capacitor-level dielectric deposition - Al metallization by sputtering (metal-1) - Hydrogen barrier: Al₂O₃ on metal-1 - Inter-metallic dielectric layers - spin-on glass - Al metallization by sputtering (metal-2)

method on a buried TiN barrier. The stack was isolated by using a conventional etching process. And then, the patterned bottom electrode was buried in the inter-layer dielectric film by an oxide chemical mechanical polishing process. A 100-nm-thick BLT thin film was deposited on the buried bottom electrode stack by the pulsed-DC sputtering method (PVD-BLT). The starting composition of the sintered BLT sputtering target was Bi_{4.8}La_{1.0}Ti_{3.0}O₁₂. The target composition was predicted with the results from a previous experiment on the MOD-BLT solution because no data based on the pulsed-DC sputtering deposition method were available for the BLT thin film. The Bi and La content in the PVD-BLT target were excessed to obtain the BLT film composition of Bi_{3.25}La_{0.75}Ti_{3.0}O₁₂, which was the optimized composition with the MOD-BLT solutions [9,11]. The process conditions for PVD-BLT layer deposition were as follows: deposition temperature of 250 °C, deposition power of 400 W, working pressure of 1.8 mTorr, and Ar/O₂ gas flow rates of 35 sccm/4 sccm. The as-deposited PVD-BLT thin film was annealed at 560 °C/O₂/6 min with rapid thermal process (RTP) to densify it. Then, the film was fully crystallized at 700 °C/O₂/30 sec with the same RTP equipment.

The crystalline orientation of the BLT film was examined by using X-ray diffraction (XRD) with a Cu-K_α radiation source. And the microstructure of the BLT films was inspected by both a scanning electron microscope (SEM) and a transmission electron microscope (TEM). Electrical properties such as contact resistance

Fig. 2. Cross-sectional scanning electron microscope image (a) and transmission electron microscope image (b) of the stacked BLT capacitor inspected after integration up to the metal-2 process. PVD-BLT: physical vapor deposition-(Bi,La)₄Ti₅O₁₂.

and ferroelectric properties of the BLT capacitors were evaluated after integration up to the metal-2 layer in accordance with the conventional process flow of a FeRAM device as described in Table 1. The ferroelectric properties such as polarization and fatigue loss were measured by using the RT6000SI ferroelectric tester (Radiant Technologies, USA).

3. RESULTS AND DISCUSSION

Thermal stability issues such as sidewall oxidation have been common in a conventional TiN barrier interposed at the interface between the oxygen barrier (Ir) and the W-plug [15]. Therefore, to obtain a robust plug structure, the buried TiN barrier was fabricated on the recessed W-plug [9]. The buried TiN barrier structure under the stacked Pt/BLT/Pt/IrO_x/Ir capacitor is shown in Fig. 2. Figure 2(a) is the cross-sectional SEM image and Fig. 2(b) is the TEM image of a novel cell structure. Sidewall oxidation was not observed even after full integration up to metallization [15].

Figure 3 shows the resistance properties of the storage node contact. Figure 3(a) is the current-voltage curve measured at one W-plug test pattern and Fig. 3(b) is the distribution of the contact resistance measured at the 1,024-contact chain pattern. The linear current-voltage relation shown in Fig. 3(a) proves the ohmic contact from the bottom electrode to the source region of the transistor. And the contact resistance values have very narrow distribution as shown in Fig. 3(b). In other words, the W-plug showed the low contact resistance of ~400 Ω/plug at Φ0.25 μm contact size.

The BLT films were deposited by the sputtering method on a buried bottom electrode stack of Pt/IrO_x/Ir. The major issue in the deposition of the BLT films to realize high polarization was the orientation control of each grain because of the strong anisotropy in electrical polarization [7,8,12]. The saturation polarization value (P_s) is small (~4 μC/cm²) along c-axis, but large (~50 μC/cm²) along a-axis or b-axis [10,12]. That is, the grain orientation in the BLT film must be aligned to the a-axis or b-axis to maximize the polarization value. However, the MOD-BLT films showed a strongly c-axis orientation, which resulted in the lowest polarization value. The c-axis orientation of the MOD-BLT films is affected by the orientation of the Pt electrode surface. And the electrode effects on the MOD-BLT films may be strongly related with the nucleation stage of the BLT grains during the

Fig. 3. Current-voltage relation of the W-plug (a) and the distribution of the contact resistance measured at 1,024-contact chain pattern (b).

Fig. 4. X-ray diffraction profile of the physical vapor deposition-BLT thin film (a) and that of the BLT powder analyzed after crystallization annealing (b). BLT: $(\text{Bi},\text{La})_4\text{Ti}_3\text{O}_{12}$.

post-annealing process performed after the spin-on coating of the MOD-BLT solution. The MOD route may follow these steps: (1) spin-on coating, (2) decomposition of the MOD solution (the Bi, La, Ti may exist as separate atoms without chemical bonding), (3) nucleation for the BLT grain, and (4) grain growth at the nuclei.

These critical orientation and grain size issues in the MOD-BLT films were the main reason for evaluating the PVD method for BLT film deposition. The crystallographic orientation of the PVD-BLT film analyzed by XRD method is shown in Fig. 4(a). As the reference in the analysis of the BLT film orientation, a specially fabricated BLT powder was also analyzed and its data is shown in Fig. 4(b). The BLT powder used as reference was fabricated as follows: (1) the BLT layer was coated on the Pt bottom electrode, (2) crystallization annealing was carried out at $700^\circ\text{C}/\text{O}_2/30\text{ sec}$, and (3) the BLT thin film was stripped off by scratching with a knife. Finally, the BLT powders containing some Pt powders were made by the soft grinding method of the stripped PVD-BLT thin film. The major diffraction peak of the PVD-BLT film was the direction of (117), which was similar to that of the reference BLT powder shown in Fig. 4(b). This similarity implies that the grains in the PVD-BLT film have a crystallographic ran-

Fig. 5. Microstructure of the physical vapor deposition-BLT thin film: (a) scanning electron microscope image of the BLT surface, (b) cross-sectional transmission electron microscope image of the BLT capacitor. BLT: $(\text{Bi},\text{La})_4\text{Ti}_3\text{O}_{12}$.

Fig. 6. Fatigue property of physical vapor deposition-BLT thin film. BLT: $(\text{Bi},\text{La})_4\text{Ti}_3\text{O}_{12}$.

dom orientation. The random orientation in the PVD-BLT thin film may be related with the nuclei generated during the deposition process. That is, the PVD-BLT films may be deposited as nano-particles, not as separated ions or atoms. Nano-particles would show random orientation regardless of the orientation on a Pt electrode surface. And they would act as nuclei of the BLT grains during the post-annealing process. That is, the PVD-BLT grains can increase in size without the nucleation step. These behaviors may be the reasons why the PVD-BLT film showed random orientation.

Recently, we reported that the orientation of the MOD-BLT film can be controlled by optimizing the post-annealing process conditions [13,14]. But, the window of the process conditions was too narrow for obtaining randomly oriented small BLT grains [13,14], which are needed for high density FeRAM devices. However, we could easily deposit PVD-BLT films having grains of random orientation, as shown in Fig. 4.

Figure 5(a) is the SEM image of the PVD-BLT surface observed after crystallization annealing at $700^\circ\text{C}/\text{O}_2/30\text{sec}$, and Fig. 5(b) is the cross-sectional TEM image of the PVD-BLT capacitor inspected after deposition on the top Pt electrode. The BLT layer has uniform, small, and ellipsoidal-shaped grains (long direction: $\sim 100\text{ nm}$, short direction: $\sim 20\text{ nm}$). The c-axis oriented large grains, which caused the failure of the cells in the real FeRAM devices fabricated with spin-coated MOD-BLT thin films [13,14], were not observed in the PVD-BLT films.

The electrical properties were measured via W-plug after integration up to metallization with aluminum. The ferroelectric hysteresis loop was obtained from 32 k-array capacitors (the number of capacitor: $32 \times 1,024$ each, unit capacitor size: $0.7\text{ }\mu\text{m}^2$). The remnant polarization (2Pr) value was about $21\text{ }\mu\text{C}/\text{cm}^2$, which was high enough for FeRAM devices. The leakage current density of the PVD-BLT capacitor was about $3 \times 10^{-5}\text{ A/}$

cm^2 at the applied voltage of 3 V. It was higher than that of the optimized MOD-BLT films [7,8]. Therefore, we analyzed the composition of the PVD-BLT layer by using the inductively coupled plasma method. The composition in the deposited PVD-BLT film was $\text{Bi}_{4.0}\text{La}_{1.0}\text{Ti}_{3.0}\text{O}_{12}$ after heat treatment. Both Bi and La contents were higher than those of the optimized MOD-BLT film, whose composition was $\text{Bi}_{3.25}\text{La}_{0.75}\text{Ti}_{3.0}\text{O}_{12}$. The excess Bi and La contents in the deposited PVD-BLT film may be the primary reason for the higher leakage current density. So, in future studies, the composition for the PVD-BLT film should be optimized by lowering the Bi and La contents in the composition of the BLT sputtering targets.

Figure 6 shows the fatigue loss of the deposited PVD-BLT film. The applied signal was 1 MHz bipolar pulse with 3V maximum voltage. The PVD-BLT film showed similar fatigue loss of about 10% after 1×10^{11} cycles as the optimized MOD-BLT film.

4. CONCLUSIONS

A stacked BLT capacitor with the novel MTP cell structure was successfully developed with the PVD-BLT thin film for a high density FeRAM device. The W-plug showed uniform low contact resistance of about 400 Ω /plug at $\Phi 0.25 \mu\text{m}$ contact size. Both microstructure and ferroelectric properties of the PVD-BLT films were also evaluated in the newly developed MTP cell structure. The PVD-BLT layer showed the random orientation in crystallographic direction and had small and ellipsoidal-shaped grains. The remnant polarization (2Pr) and the leakage current density were about 21 $\mu\text{C}/\text{cm}^2$ and $3 \times 10^{-5} \text{ A}/\text{cm}^2$ at 3 V, respectively. The fatigue loss was about 10% of the initial polarization value after 1×10^{11} fatigue cycles. In conclusion, the PVD-BLT film is a very promising candidate as a ferroelectric layer for high density FeRAM devices because its small grains in random orientation can be easily deposited by the pulsed-DC sputtering method.

ACKNOWLEDGMENTS

The research was supported by the Regional Innovation Center (RIC) Program, which was conducted by the Ministry of Commerce, Industry and Energy of the Korean Government.

REFERENCES

- [1] J. F. Scott and C. A. Paz de Araujo, *Science* **246**, 1400 (1989) [<http://dx.doi.org/10.1126/science.246.4936.1400>].
- [2] C. A. P. de Araujo, J. D. Cuchiaro, L. D. McMillan, M. C. Scott, and J. F. Scott, *Nature* **374**, 627 (1995) [<http://dx.doi.org/10.1038/374627a0>].
- [3] B. H. Park, B. S. Kang, S. D. Bu, T. W. Noh, J. Lee, and W. Jo, *Nature* **401**, 682 (1999) [<http://dx.doi.org/10.1038/44352>].
- [4] Y. J. Son, Y. J. Kim, B. H. Lee, S. Y. Hwang, N. K. Park, H. Y. Chang, S. K. Hong, S. J. Hong, J. H. Choi, and S. Y. Kweon, *J. Korean Phys. Soc.* **51**, 701 (2007).
- [5] S. H. Park, Y. J. Son, S. S. Cho, S. Y. Hwang, A. K. Lee, H. C. Park, S. K. Hong, S. J. Hong, M. H. Kang, S. K. Lim, W. G. Lee, J. H. Choi, and S. Y. Kweon, *J. Korean Phys. Soc.* **51**, 710 (2007).
- [6] S. K. Hong, Y. J. Son, Y. J. Kim, Y. W. Song, and S. Y. Kweon, *J. Korean Phys. Soc.* **55**, 869 (2009).
- [7] B. Yang, Y. M. Kang, S. S. Lee, K. H. Noh, S. W. Lee, N. K. Kim, S. Y. Kweon, S. J. Yeom, and Y. J. Park, *IEEE Electron Device Lett.* **23**, 743 (2002) [<http://dx.doi.org/10.1109/led.2002.806299>].
- [8] N. K. Kim, S. J. Yeom, S. Y. Kweon, E. S. Choi, H. J. Sun, J. S. Roh, H. C. Sohn, D. W. Lee, H. S. Kim, B. H. Choi, J. W. Kim, K. J. Choi, N. J. Seong, and S. G. Yoon, *Appl. Phys. Lett.* **85**, 4118 (2004) [<http://dx.doi.org/10.1063/1.1812840>].
- [9] S. Y. Kweon, N. K. Kim, E. S. Choi, S. J. Yeom, J. S. Roh, and Y. J. Park, *Jpn. J. Appl. Phys.* **41**, 7327 (2002) [<http://dx.doi.org/10.1143/JJAP41.7327>].
- [10] S. E. Cummins and L. E. Cross, *J. Appl. Phys.* **39**, 2268 (1968) [<http://dx.doi.org/10.1063/1.1656542>].
- [11] S. J. Yeom, W. S. Yang, N. K. Kim, S. Y. Kweon, E. S. Choi, and J. S. Roh, *Jpn. J. Appl. Phys.* **42**, L182 (2003) [<http://dx.doi.org/10.1143/JJAP42.L182>].
- [12] B. Yang, S. S. Lee, Y. M. Kang, K. H. Noh, S. W. Lee, N. K. Kim, S. Y. Kweon, S. J. Yeom, and Y. J. Park, *Jpn. J. Appl. Phys.* **42**, 1327 (2003) [<http://dx.doi.org/10.1143/JJAP42.1327>].
- [13] Y. M. Kim, G. E. Jang, N. K. Kim, S. J. Yeom, and S. Y. Kweon, *Master. Sci. Forum*, **544-545**, 577 (2007) [<http://dx.doi.org/10.4028/www.scientific.net/MSE544-545.577>].
- [14] N. K. Kim, S. J. Yeom, S. K. Hong, and H. B. Kang, *J. Korean Phys. Soc.* **58**, 132 (2011).
- [15] E. S. Choi, N. K. Kim, S. Y. Kweon, H. J. Sun, S. J. Yeom, J. G. Kim, J. S. Roh, J. W. Kim, and Y. J. Park, *Integr. Ferroelectr.* **66**, 107 (2004) [<http://dx.doi.org/10.1080/10584580490894861>].