Low Power Test for SoC(System-On-Chip)

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Abstract—Power consumption during testing System-On-Chip (SOC) is becoming increasingly important as the IP core increases in SOC. We present a new algorithm to reduce the scan-in power using the modified scan latch reordering and clock gating. We apply scan latch reordering technique for minimizing the hamming distance in scan vectors. Also, during scan latch reordering, the don't care inputs in scan vectors are assigned for low power. Also, we apply the clock gated scan cells. Experimental results for ISCAS 89 benchmark circuits show that reduced low power scan testing can be achieved in all cases.

Index Terms—SoC, low power test, scan circuit

I. INTRODUCTION

THE SoC(System-On-chip) revolution has brought some new challenges to both design and test engineers. Among these challenges, the power dissipation is one of the most important issues[1]. In [2], a survey on low power testing is given which classifies the recent techniques into low power external test and low power BIST(Built In Self Test). In this paper, we focus on the scan based design that belongs to the external test category[2].

The power of digital system is considerably higher in test mode than in normal mode. The reason is that test patterns cause as many nodes switching as possible while normal mode only activates a few modules at the same time. Special care must be taken to ensure that the power consumption is not exceeded during test application.

A new ATPG tool[3] was proposed to overcome the low correlation between consecutive test vectors during test application. The methods about low power mapping and test compression for unspecified scan vectors were proposed[4,5]. Also, a new compression and low power consumption technique using Scan Latch Reordering(SLR) was proposed[6,7]. It mapped the don't care input for low power and performed the SLR[8].

II. POWER CONSUMPTION MODEL

A. Power Consumption Model

Power dissipation in CMOS circuits can be classified into static, short circuit, leakage and dynamic power dissipation. The static power is negligible. The short circuit power dissipation caused by short circuit current and power dissipated by leakage currents contribute up to 20% of the total power dissipation. The remaining 80% is attributed to dynamic power dissipation caused by switching of the gate outputs. If the gate is part of a synchronous digital circuit controlled by global clock, it follows that the dynamic power $P_d$ required to charge and discharge the output capacitance load of every gate is:

$$P_d = 0.5C_{load}V_{dd}^2F_cN_g$$

where $C_{load}$ is the load capacitance, $V_{dd}$ is the supply voltage, $F_c$ is the global clock frequency, and $N_g$ is the total number of gate output transitions.

These transitions are major factor of power dissipation. The power dissipation during full-scan testing is due to the dynamic power by transitions occurred when the scan vectors are shifted in the scan chain. These transitions are major factor of power dissipation. The power dissipation during full-scan testing is due to the dynamic power by transitions occurred when the scan vectors are shifted in the scan chain.

B. Scan-in Power Model

Power consumption in testing a sequential circuit with a single scan chain includes; a scan-in power consumed during the scan-in operations of scan vectors, scan-out power consumed during the scan-out operations of test
response and a power consumed in combinational logic of the sequential circuit. It is difficult to estimate the scan-out power directly from the scan vector set since the test response must be determined from the function of the core under test. We consider the scan-in power only and measure it in terms of Weighted Transition Metric (WTM).

The scan-in power depends not only on the number of transitions in it but also on their relative positions. For example, consider the scan vector \( S_1 S_2 S_3 S_4 S_5 = 10101 \) with scan length 5. If the left most bit \( S_1 \) is first shifted in the scan chain, the transition of \( (S_1, S_2) \) causes four (scan length -1) transitions during scan-in. Therefore, the transition of \( (S_j, S_{j+1}) \) causes \( (\text{scan length} - j) \) transitions.

Let each scan vector \( SV \) with scan length \( k \) be \( S_1 S_2 \ldots S_k \). The scan-in power for \( SV \) is given by

\[
P_{SV} = WTM(SV) = \sum_{j=1}^{k-1} (S_j \oplus S_{j+1})(k - j)
\]

Also, assuming that the set of scan vector used for testing is \( SV_{set}=SV_1 SV_2 \ldots SV_n \), the power consumed during scan-in of \( SV_{set} \) is

\[
WTM(SV_{set}) = \sum_{i=1}^{n} WTM(SV_i)
\]

Therefore, the average power consumption and peak power consumption can be represented such as below.

\[
P_{avg} = \frac{WTM(SV_{set})}{n}
\]
\[
P_{peak} = \text{Max}(WTM(SV_i))
\]

III. SCAN LATCH REORDERING AND CLOCK GAING

A. Cost function for scan latch reordering

Let's denote \( SV_{set} \) be \( SV[r][c] \) of two dimensional array, whose number of scan vector is \( r \) and input number of scan vector is \( c \). Each element of array, \( SV[i][j] \) means the \( j^{th} \) scan input of the \( i^{th} \) scan vector.

The WTM(\( SV_{set} \)) is described as below.

\[
WTM(SV_{set}) = \sum_{i=1}^{r} \sum_{j=1}^{c} (SV[i][j] \oplus SV[i][j+1])(c - j)
\]

\[
= \sum_{j=1}^{c-1} \sum_{i=1}^{r} (SV[i][j] \oplus SV[i][j+1])(c - j)
\]

\[
= \sum_{j=1}^{c-1} HD_{col}(j, j+1)(c - j)
\]

In above equation, we can define the \( HD_{col}(j,j+1) \) as the hamming distance between \( j^{th} \) column and \( (j+1)^{th} \) column for all rows. In order for WTM(\( SV_{set} \)) to be small, the HD col must be small. The scan latch reordering means the reordering of column position in scan vectors. Therefore, it will be good to use the column hamming distance as the cost function of scan latch reordering.

B. Clock gating

The clock signal is a major source of dynamic power dissipation. The clock gating have become a popular way to reduce the transition in sequential circuit. Also, There are many F/Fs in scan chains. The power consumption during scan-in can be reduced by clock gating in scan cells because the scan cells have the same logic value during scan test.

C. Proposed Algorithm

\( HD_{col}(j,j+1) \) is the Hamming Distance of between column \( j \) and \( j+1 \), and calculate it considering don't care input.

Given \( SV[i][j] \in \{0,1,X(\text{don't care input})\} \), the hamming distance between \( SV[i][j] \) and \( SV[i][j+1] \) is 1 only in the condition that \( (SV[i][j], SV[i][j+1]) \) is \((0,1) \) or \((1,0) \). In case of \((0,X) \) and \((1,X) \), the hamming distance becomes 0 because the value of \( SV[i][j] \) can be assigned to \( X \) existing in \( SV[i][j+1] \).

Because scan latch reordering is a NP-hard problem, it is very difficult to find near optimal solution. We propose Heuristic algorithm below.

- Define \( SV[*][j] \) as \( j^{th} \) column in two dimensional array of scan vectors.
- Initialize arbitrary \( SV[*][j] \) to \( SV[*][1] \). And assign 0 to all X within \( SV[*][1] \).
- Choose minimized \( j \) after calculating Hamming Distance about \( SV[*][1] \) and all \( SV[*][j] \). And exchange \( SV[*][2] \) and \( SV[*][j] \). The transition of \( SV[*][1] \) and \( SV[*][2] \) becomes the minimum.
- By assigning the value of \( SV[*][2] \) existing in the same row to \( X \) within \( SV[*][1] \), prevent the transition from occurring.

In this way, carry out reordering about all \( SV[*][j] \) to make Hamming Distance the minimum.

The proposed algorithm can be described by pseudo code at Figure 2.
IV. EXPERIMENTAL RESULTS

In this section, we evaluate the effect of the proposed method in power consumption during scan testing for ISCAS89 benchmark circuits. The experiments were conducted on a Sun Ultra 10 workstation.

We considered full-scan sequential circuits. For each full-scan circuit, we assumed a single scan chain for our experiments. We used partially-specified scan vector sets generated by MINTEST Automatic Test Pattern Generation (ATPG) program with dynamic compaction [9].

In the column compression ratios, sub column 0 Mapping maps only 0 to don't care inputs [4]. The MTC Map & SLR is the proposed method in [8].

Table I shows the reduction ratios for peak power. The power consumption in our method is reduced to 37% less than MTC Map & SLR in case of s5378. Also, the power consumption in our method is reduced to 73% less than MTC Map & SLR in case of s38417. The experimental results show that the proposed method has a better reduction ratio than previous method.

V. CONCLUSIONS

As the number of the IP core increases in the SOC, test data volume and testing time increase too. As a result, the testing and chip costs go up and productivity goes down. Also, power consumption in test mode is much larger than that in normal mode and causes damage on chip due to excessive power consumption.

This paper proposes a new algorithm that has efficient low power for unspecified scan vectors. It applies mapping don't care input at the same time of performing scan latch reordering using the hamming distance as the cost function. The proposed method shows power reduction as compared to the previous method.

REFERENCES


TABLE I
REDUCTION RATIOS FOR PEAK POWER

<table>
<thead>
<tr>
<th>Circuit</th>
<th>0 Mapping</th>
<th>MTC Map &amp; SLR</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Peak</td>
<td>Peak</td>
<td>Peak</td>
</tr>
<tr>
<td>S5378</td>
<td>10127</td>
<td>5556</td>
<td>3464</td>
</tr>
<tr>
<td>S9234</td>
<td>12994</td>
<td>7400</td>
<td>4798</td>
</tr>
<tr>
<td>S13207</td>
<td>101127</td>
<td>35486</td>
<td>11327</td>
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<tr>
<td>S15850</td>
<td>81832</td>
<td>33207</td>
<td>12131</td>
</tr>
<tr>
<td>S38417</td>
<td>505295</td>
<td>181436</td>
<td>48631</td>
</tr>
<tr>
<td>S38584</td>
<td>531321</td>
<td>187379</td>
<td>100319</td>
</tr>
</tbody>
</table>

The reduction ratio is about 5692 in 0 Mapping, 7703 in MTC&SLR in the case of s13207. The proposed method gives a good result of 766, which it shows about 90% less than MTC&SLR in this case.

As showed in above experimental results, the proposed method has higher power reduction ratios.

TABLE II
REDUCTION RATIOS FOR AVERAGE POWER

<table>
<thead>
<tr>
<th>Circuit</th>
<th>0 Mapping</th>
<th>MTC Map &amp; SLR</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Avg</td>
<td>Avg</td>
<td>Avg</td>
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</table>

The reduction ratio is about 5692 in 0 Mapping, 7703 in MTC&SLR in the case of s13207. The proposed method gives a good result of 766, which it shows about 90% less than MTC&SLR in this case.

As showed in above experimental results, the proposed method has higher power reduction ratios.

REFERENCES


Fig. 2. Proposed Algorithm

SV_set = SV[r][c];
Initialize SV[*][1]; /* Initialization of SV[*][1] to arbitrary SV[i][j]. */
For(j=1; j<c; j++)
{
  for(k=j+1; k<c+1; k++)
    HD_col(j,k); /* Calculate HD_col */
  Search the index k with minimum HD_col;
  Exchange the column j+1 with column k;
}
HD_col(j,k)
{ HD_sum(k) = 0;
  for( i =1; i<r+1; i++)
    if( (SV[i][j] == 0 & & SV[i][k] == 1) | 
        SV[i][j] == 1 & & SV[i][k] == 0 )
      HD_sum(k)++;
}
  Apply Clock gating


**Jun-Mo Jung** received the Ph. Degree from Hanyang University in 2004, and is currently a professor at Dept. of Electronic Engineering at Kunsan National University, worked as a visiting Professor at Queensland Micro -technology Facility at Griffith University in Australia in 2009–2010. His research areas include ASIC design, Digital Signal Processing and NoC test.