Analysis and Implementation of a DC-DC Converter with an Active Snubber

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Abstract

This paper presents a soft switching converter to achieve the functions of zero voltage switching (ZVS) turn-on for the power switches and dc voltage step-up. Two circuit modules are connected in parallel in order to achieve load current sharing and to reduce the size of the transformer core. An active snubber is connected between two transformers in order to absorb the energy stored in the leakage and magnetizing inductances and to limit the voltage stresses across the switches. During the commutation stage of the two complementary switches, the output capacitance of the two switches and the leakage inductance of the transformers are resonant. Thus, the power switches can be turned on under ZVS. No output filter inductor is used in the proposed converter and the voltage stresses of the output diodes is clamped to the output voltage. The circuit configuration, the operation principles and the design considerations are presented. Finally, laboratory experiments with a 340W prototype, verifying the effectiveness of the proposed converter, are described.

Key Words: DC Converter, Soft Switching

I. INTRODUCTION

In order to help mitigate climate changes and environmental pollution, the Environment Protection Agency (EPA) and the Climate Saver Computing Initiative (CSCI) have proposed efficiency requirements for modern power supply units. DC-DC [1]–[9] converters with zero voltage switching (ZVS), have been proposed with advantages such as high frequency operation, ZVS or zero current switching (ZCS) switching and high circuit efficiency. However, the voltage stresses or current stresses in the resonant converters are much to high for high input voltage or current applications. Active snubbers [10]–[12] have been presented to reduce voltage spikes and switching losses and to increase circuit efficiency. Power switches are turned on under ZVS during the transition interval based on the transformer leakage inductance and the switch output capacitance. However, a high power rating and a high power density are required in many practical applications such as computer servers and telecommunication power supplies. One way to increase output power is to connect two or more converter cells in parallel. Thus the current stresses and the power losses can be distributed among all of the converter cells. An interleaved PWM controller can control several converter cells with a phase-shifted PWM technique to realize load current sharing and ripple current cancellation. Parallel forward converters with soft switching techniques have been presented in [13]–[15] to realize ZVS operation and to achieve conversion efficiency improvements. However, the control schemes are more difficult to implement and many switches are used in the circuits.

This paper presents a parallel soft switching converter with an output voltage doubler topology. Two circuit modules with the same power switches are connected in parallel at the input and output sides to reduce the current stresses on the output diodes and the primary and secondary windings of the transformers. An active snubber is connected between two power transformers to achieve a transformer flux reset, to limit the voltage spikes on power switches and to achieve the ZVS turn-on of switches. In the secondary side, an output voltage doubler is used to achieve an output voltage step-up. The circuit configuration, operation principles, mathematical analysis and design considerations of the proposed converter are analyzed in detail. Experiments based on a 340W laboratory prototype are presented to verify the circuit performance.

II. CIRCUIT CONFIGURATION

The circuit configuration of the proposed converter is shown in Fig. 1. There are two modules connected in parallel to share the load current. \( V_{in} \) is the input voltage, \( T_1 \) and \( T_2 \) are the isolated transformers, \( L_1 \) and \( L_2 \) are the resonant inductances, \( L_{m1} \) and \( L_{m2} \) are the magnetizing inductances, and \( S_1 \) and \( S_2 \) are the main and auxiliary switches. \( D_{S1} \) and \( D_{S2} \) are the anti-parallel diodes of \( S_1 \) and \( S_2 \), respectively. An active snubber including \( S_2 \) and \( C_c \) is connected between the two transformers \( T_1 \) and \( T_2 \) to limit the voltage stress of the power switches \( S_1 \) and \( S_2 \) and to implement the flux reset of \( T_1 \) and \( T_2 \). During the transition interval of \( S_1 \) and \( S_2 \), the capacitors \( C_{S1} \) and \( C_{S2} \)
and the inductors $L_1$ and $L_2$ are resonant to allow the ZVS turn-on feature on the switches $S_1$ and $S_2$. Thus, the switching losses and the thermal stresses of the semiconductors and the transformers are reduced. In the secondary side of $T_1$ and $T_2$, a voltage doubler rectifier is used to obtain a stable output voltage $V_o$. The PWM signals of $S_1$ and $S_2$ are complementary to each other with a small delay time which can be generated from a general PWM IC or from an active clamp PWM IC with an isolated gate driver.

III. OPERATION PRINCIPLE

Based on the on and off states of the switches $S_1$ and $S_2$ and the diodes $D_1$–$D_4$, there are six operating modes in the proposed converter during one switching cycle. Fig. 2 shows the key waveforms of the proposed converter and Fig. 3 gives the topological operating modes in a switching cycle. Before the system analysis, the following assumptions are made:

- $\delta$ is a duty cycle of the main switch $S_1$;
- The conduction times of $S_1$ and $S_2$ are $\delta T_s$ and $(1-\delta)T_s$, where $T_s$ is the switching period;
- The capacitances $C$, $C_c$, $C_{o1}$ and $C_{o2}$ are much larger such that the voltages $V_C$, $V_{Cc}$, $V_{o1}$ and $V_{o2}$ are assumed to be constant;
- The capacitances $C_{S1}$ and $C_{S2}$ are less than the capacitances $C$ and $C_c$;
- The turns ratio of $T_1$ and $T_2$ are identical $n=n_{T1}=n_{T2}=n_p/n_s$;
- The resonant inductances $L_{1r}=L_{2r}=L_r$ are much less than the magnetizing inductances $L_{m1}=L_{m2}=L_m$;
- In the steady state, the average capacitor voltage $V_C=V_{in}$. Before time $t_0$, the switch $S_1$ is in the on-state. Since the inductor current $i_{Lr1}+i_{Lm1}$ and the inductor current $i_{Lr2}+i_{Lm2}$, the secondary winding current $i_{T1s}$ is negative and the secondary winding current $i_{T2s}$ is positive, respectively. Thus, the diodes $D_2$ and $D_4$ are conducting. The primary voltage $v_{Lm1}=nV_{o1}$ and the primary voltage $v_{Lm2}=nV_{o2}$. The inductor current $i_{Lr1}$ increases and the inductor current $i_{Lr2}$ decreases.

**Mode 1 $[t_0 \leq t < t_1]$** At time $t_0$, the inductor current $i_{Lr1}>i_{Lm1}$ and the inductor current $i_{Lr2}<i_{Lm2}$, respectively. Thus the diodes $D_1$ and $D_3$ are conducting in this mode. The primary voltage $v_{Lm1}=nV_{o1}$ and the primary voltage $v_{Lm2}=nV_{o2}$. Since the switch $S_1$ is in the on-state, the inductor currents $i_{Lr1}$ and $i_{Lr2}$ are expressed as:

$$i_{Lr1}(t) \approx i_{Lr1}(t_0) + \frac{V_{in} - nV_{o1}(t-t_0)}{L_r}$$

$$i_{Lr2}(t) \approx i_{Lr2}(t_0) + \frac{nV_{o1} - V_C}{L_r}(t-t_0).$$

Since $V_{in}>nV_{o1}$, the inductor current $i_{Lr1}$ increases and the inductor current $i_{Lr2}$ decreases. The magnetizing currents $i_{Lm1}$ and $i_{Lm2}$ are given as:

$$i_{Lm1}(t) = i_{Lm1}(t_0) + nV_{o1}(t-t_0)/L_m$$

$$i_{Lm2}(t) = i_{Lm2}(t_0) - nV_{o1}/L_m(t-t_0).$$

Power is delivered from the input terminal voltage $V_{in}$ to the output capacitor $C_{o1}$ through $T_1$, $S_1$ and $D_1$. The energy stored in the capacitor $C$ also delivers power to the capacitor $C_{o1}$ through $T_2$, $S_1$ and $D_3$. The secondary diode currents $i_{D1}$ and $i_{D3}$ are given as:

$$i_{D1}(t) = n(i_{Lr1}(t) - i_{Lm1}(t))$$

$$i_{D3}(t) = n(i_{Lm2}(t) - i_{Lr2}(t)).$$

The switch current $i_{S1}$ is expressed as:

$$i_{S1}(t) = i_{Lr1}(t) - i_{Lr2}(t)$$

$$\approx i_{Lr1}(t_0) - i_{Lr2}(t_0) + \frac{2(V_{in} - nV_{o1})(t-t_0)}{L_r}.$$  

This mode ends at time $t_1$ when $S_1$ is turned off.

**Mode 2 $[t_1 \leq t < t_2]$** At time $t_1$, $S_1$ is turned off. $C_{S1}$ is charged from the zero voltage and $C_{S2}$ is discharged from $V_{in}+V_C-V_{Cc}$. The components $L_{r1}$, $L_{r2}$, $C_{S1}$ and $C_{S2}$ are resonant in this mode. Since the time interval in this mode is negligible when compared to the switching period $T_s$, the primary currents $i_{Lr1}$ and $i_{Lr2}$ are almost constant and $C_{S1}$ and $C_{S2}$ are linearly charged and discharged, respectively. The diodes $D_1$ and $D_3$ are still conducting in this mode. At time $t_2$, the capacitor voltage $v_{CS1}$ decreases to zero and the capacitor voltage $v_{CS2}$ increases to $V_{in}+V_C-V_{Cc}$. When the voltage $v_{S2,ds}$
(or $v_{CS2}$) becomes zero at time $t_2$, the anti-parallel diode $D_{S2}$ of the switch $S_2$ is conducting.

**Mode 3 [$t_2 \leq t < t_3$]:** At time $t_2$, the anti-parallel diode $D_{S2}$ is conducting and the switching current $i_{S2}$ is negative. Thus the switch $S_2$ can be turned on in this mode to realize ZVS. Since the diodes $D_1$ and $D_3$ are still conducting in this mode, the magnetizing current $i_{Lm1}$ increases and the magnetizing current $i_{Lm2}$ decreases, respectively. The inductor voltage $v_{L1} = v_{Cc} - v_{Cn} < 0$ and the inductor voltage $v_{L2} = n v_{o1} + v_{in} V_C > 0$. Therefore, the inductor current $i_{L1}$ decreases and the inductor current $i_{L2}$ increases. At time $t_3$, $i_{L1} = i_{Lm1}$ and $i_{L2} = i_{Lm2}$. Then the diodes $D_1$ and $D_3$ are off and the diodes $D_2$ and $D_4$ are conducting.

**Mode 4 [$t_3 \leq t < t_4$]:** In this mode, $i_{L1} < i_{Lm1}$ and $i_{L2} > i_{Lm2}$. Thus the diodes $D_1$ and $D_3$ are off and the diodes $D_2$ and $D_4$ are conducting. The auxiliary switch $S_2$ is still in the on-state. The magnetizing voltage $v_{Lm1} = n v_{o2}$ and the magnetizing voltage $v_{Lm2} = n v_{o2}$. Thus the magnetizing current $i_{Lm1}$ decreases and the magnetizing current $i_{Lm2}$ increases, respectively. The inductor voltage $v_{L1} = v_{Cc} + n v_{o2} V_C < 0$ and the inductor voltage $v_{L2} = V_{in} V_C - n v_{o2} > 0$. Thus the inductor current $i_{L1}$ decreases and the inductor current $i_{L2}$ increases.

The power is transferred from the input terminal $V_{in}$ to the output capacitor $C_{o2}$ through $S_2$, $C_r$, $L_r$, $T_2$, $D_4$, and $C_{o2}$. The switch current $i_{S2} = i_{L2} - i_{L1}$. This mode ends at time $t_4$ when $S_2$ is turned off.

**Mode 5 [$t_4 \leq t < t_5$]:** At time $t_4$, the auxiliary switch $S_2$ is turned off. Since $i_{L2} (t_4) - i_{L1} (t_4) < 0$, the capacitor $C_{S2}$ is charged and the capacitor $C_{S1}$ is discharged. The drain voltage $V_{S1,d}$ decreases from $V_{in} + V_C V_{Cc}$ and the drain voltage $V_{S2,d}$ increases from zero voltage. Since the time interval in this mode is negligible when compared to the switching period $T_s$, the inductor currents $i_{L1}$ and $i_{L2}$ are almost constant and $C_{S1}$ and $C_{S2}$ are linearly discharged and charged, respectively. The diodes $D_2$ and $D_4$ are still conducting in this mode. At time $t_5$, the capacitor voltage $V_{CS2}$ decreases to zero and the capacitor voltage $V_{CS2}$ increases to $V_{in} + V_C V_{Cc}$. When the voltage $V_{CS1,ds}$ (or $V_{CS1}$) becomes zero at time $t_5$, the anti-parallel diode $D_{S1}$ of switch $S_1$ is conducting.

**Mode 6 [$t_5 \leq T < T_0$]:** At time $t_5$, the anti-parallel diode $D_{S1}$ is conducting and the switching current $i_{S1}$ is negative. Thus the switch $S_1$ can be turned on at this instant to achieve ZVS. Since the diodes $D_2$ and $D_4$ are still conducting in this mode, the magnetizing current $i_{Lm1}$ decreases and the magnetizing current $i_{Lm2}$ increases. The inductor voltage $v_{L1} = V_{in} + n v_{o2} > 0$ and the inductor voltage $v_{L2} = -n v_{o2} V_C < 0$. Therefore, the inductor current $i_{L1}$ increases and the inductor current $i_{L2}$ decreases. At time $T + t_0$, $i_{L1} = i_{Lm1}$ and $i_{L2} = i_{Lm2}$. Then the diodes $D_2$ and $D_4$ are off, and the diodes $D_1$ and $D_3$ are conducting. Then, the circuit operation of the proposed converter in a switching cycle is completed.

**IV. Circuit Analysis**

The transition intervals in modes 2 and 5 are much shorter than the other time intervals. Thus these two modes to derive the dc voltage conversion ratio of the proposed converter were neglected. In mode 1, $S_1$ is on. The time interval in this mode is $(\delta - \delta_6) T_s$, where $\delta$ is the duty cycle of $S_1$, $\delta_6$ is the duty loss in mode 6, and $T_s$ is the switching period. The voltages on $L_m1$ and $L_m2$ are $-n V_{o1}$ and $-n V_{o1}$. Thus the inductor voltage $v_{L1} = V_{in} - n V_{o1}$ and the inductor voltage $v_{L2} = -n V_{o1} - v_{in} V_C$. In mode 3, $S_2$, $D_1$ and $D_3$ are on such that $v_{Lm1} = -n V_{o1}$, $v_{Lm2} = -n V_{o1}$, $v_{L1} = v_{Cc} V_{Cc} - n V_{o1}$ and $v_{L2} = V_{in} + n V_{o1} V_C$. The time interval in this mode is $\delta_3 T_s$. In mode 4, $S_2$, $D_2$ and $D_4$ are on such that $v_{Lm1} = -n V_{o2}$, $v_{Lm2} = -n V_{o2}$, $v_{L1} = V_C V_{Cc}$ and $v_{L2} = V_{in} - n V_{o2} V_C$. The time interval in this mode is $\delta_6 T_s$. Based on the voltage-second balance on the secondary windings of $T_1$ and $T_2$, the output capacitor voltages are given as:

$$v_{o1} = (1 - \delta - \delta_3 - \delta_6) V_o$$

$$v_{o2} = (\delta + \delta_3 + \delta_6).$$

Based on the volt-second balance on the inductors $L_{r1}$ and $L_{r2}$ and the inductors $L_{m1}$ and $L_{m2}$, the voltages $V_{Cc}$ and $V_C$ of capacitors $C_r$ and $C$ are expressed as:

$$V_{Cc} = (1 - 2 \delta) V_{in} / (1 - \delta)$$

$$V_C = V_{in}.$$

The voltage conversion ratio $M$ of the proposed converter can be expressed as:

$$M = \frac{V_o + V_f}{V_{in}} \approx \frac{1}{n (1 - \delta - \delta_3 - \delta_6) (1 + L_r/L_m)}$$

$$\approx \frac{1}{n (1 - \delta - \delta_3 - \delta_6)}$$

where $V_f$ is the voltage drop on the diodes $D_1 \sim D_4$. The peak diode current $i_{D2,peak}$ can be expressed as:

$$i_{D2,peak} = I_o / (1 - \delta - \delta_3 + \delta_6).$$

The duty cycle loss in mode 6 can be obtained by the diode current $i_{D2}$ from the peak diode current $i_{D2,peak}$ to zero.

$$i_{D2,peak} \approx \frac{V_{in} + n V_{o2} (\delta + \delta_3 - \delta_6)}{L_r}.$$

If $\delta_3 + \delta_6$ is assumed, then the duty cycle loss $\delta_6$ can be obtained from (13) and (14).

$$\delta_6 = \frac{I_o L_r f_s}{n (V_{in} + n V_{o2} [\delta + \delta_3 - \delta_6]) (1 - \delta)}.$$

Based on the assumption of $\delta_3 = \delta_6$, the following equations can be obtained from (8)-(13).

$$V_{o1} \approx (1 - \delta) V_o$$

$$V_{o2} \approx \delta V_o$$

$$M = \frac{V_o + V_f}{V_{in}} \approx \frac{1}{n (1 - \delta)}$$

$$i_{D2,peak} \approx i_{D4,peak} \approx I_o / (1 - \delta)$$

$$i_{D1,peak} \approx i_{D3,peak} \approx I_o / \delta.$$
are equal to $V_o+V_f$. To meet the current-second balance for $C$ and $C_c$, the dc magnetizing currents $i_{mn1,av}$ of $T_1$ and $i_{mn2,av}$ of $T_2$ are given as:

$$i_{mn1,av} = \frac{I_o}{n(1-\delta)} \tag{21}$$

$$i_{mn2,av} = 0. \tag{22}$$

The ripple components of $i_{mn1}$ and $i_{mn2}$ are expressed as:

$$\Delta i_{mn1} = \frac{nV_{o1}}{L_m}(\delta - \delta_0)T_s \approx \frac{n\delta(1-\delta)V_oT_s}{L_m} \tag{23}$$

$$\Delta i_{mn2} \approx \frac{n\delta(1-\delta)V_oT_s}{L_m}. \tag{24}$$

The peak and root-mean-square (rms) values of the switching currents can be expressed as:

$$i_{s1,\text{rms}} \approx \sqrt{\frac{\delta}{n(1-\delta)}} + \delta \left(\frac{n\delta(1-\delta)V_oT_s}{L_m}\right)^2 + \delta \left(\frac{I_o}{12}\right)^2 \tag{26}$$

$$i_{s2,\text{rms}} \approx \sqrt{\frac{1}{3} \left(\frac{n\delta(1-\delta)V_oT_s}{L_m}\right)^2 + \frac{1-\delta}{12} \left(\frac{I_o}{1-\delta}\right)^2}. \tag{27}$$

The voltage stresses of $S_1$ and $S_2$ can be obtained from modes 4 and 1.

$$V_{s1,\text{stress}} = V_{s2,\text{stress}} = V_{in} + V_C - V_{Cc} \approx \frac{V_m}{1-\delta}. \tag{28}$$

From (28), it can be seen that the voltage stresses of $S_1$ and $S_2$ are related to the input voltage $V_{in}$ and the duty cycle $\delta$. Basically, the ZVS condition of the main switch $S_1$ is more difficult to realize than that of the auxiliary switch $S_2$. Thus only the ZVS condition of the switch $S_1$ is considered. At time $t_4$, the inductor currents $i_{Lr1}(t)$ and $i_{Lr2}(t)$ are approximately given as:

$$i_{Lr1}(t_4) \approx -n\delta(1-\delta)V_oT_s/(2L_m) \tag{29}$$
Analysis and Implementation of a DC-DC Converter with an Active Snubber

Fig. 4. Measured waveforms of gate voltage, drain voltage and switch current of switch S1 at (a) 30% load (b) 60% load (c) 100% load.

\[ i_{Lr2}(t_4) \approx \frac{n\delta(1-\delta)V_{io}T_s}{2L_m} + \frac{I_o}{n(1-\delta)}. \]  
(30)

To ensure the ZVS turn-on of the switch S1, the energy stored in the inductors \( L_{r1} \) and \( L_{r2} \) must be greater than the energy stored in the capacitors \( C_{S1} \) and \( C_{S2} \) in mode 4. Thus the ZVS condition of \( S_1 \) is expressed as:

\[ L_r(i_{Lr1}(t_4) + i_{Lr2}(t_4)) \geq C_{S1}V_{C1}^2/(1-\delta)^2. \]  
(31)

Thus the minimum inductance \( L_r \) is expressed in (32) to realize the ZVS turn-on of \( S_1 \).

\[ L_r \geq \frac{C_{S1}V_{C1}^2/(1-\delta)^2}{(\frac{n\delta(1-\delta)V_{io}T_s}{2L_m})^2 + (\frac{n\delta(1-\delta)V_{io}T_s}{2L_m} + \frac{I_o}{n(1-\delta)})^2}. \]  
(32)

V. EXPERIMENTAL RESULTS

A laboratory prototype circuit with a 340W (200V/1.7A) rated power was built to verify the effectiveness of the proposed converter. The nominal input terminal voltage \( V_{in} \) is 48V and the minimum and maximum input voltages are 36V and 60V, respectively. The proposed converter is operated at a switching frequency \( f_s = 70kHz \). An EI-40 core was used for the transformers \( T_1 \) and \( T_2 \). The primary winding turns \( N_p \) are 18 and the secondary winding turns \( N_s \) are 50. The

The peak-to-peak ripple current on \( C \) is given as:

\[ \Delta i_C \approx \Delta i_{Lr2} + I_o/(n\delta). \]  
(33)

If the ripple capacitor voltage \( \Delta V_C \) is given, then the capacitance of \( C \) can be obtained as:

\[ C \approx \Delta i_C \delta T/\Delta V_C. \]  
(34)

Fig. 5. Measured waveforms of gate voltage, drain voltage and switch current of switch S2 at (a) 30% load (b) 60% load (c) 100% load.
magnetizing inductances $L_m$ of $T_1$ and $T_2$ are 100mH. The resonant inductances of $L_{r1}$ and $L_{r2}$ are 10mH. The output filter capacitances $C_{o1}$ and $C_{o2}$ are 330mF/420V. IRFP264N MOSFETs are used for the switches $S_1$ and $S_2$ and ER605 fast recovery diodes are adopted for the diodes $D_1$-$D_4$.

The capacitances of $C_{r}$ and $C$ are 16mF. A type II voltage controller was adopted to regulate the output voltage using IC UCC2893 PWM control. Fig. 4 shows the measured gate voltage $v_{S1,g}$, the drain voltage $v_{S1,d}$ and the switch current $i_{S1}$ of the switch $S_1$ at 30%, 60% and 100% load conditions, respectively. Before the switch $S_1$ is turned on, the switch current $i_{S1}$ is negative to discharge the capacitor $C_{S1}$. Thus the drain voltage $v_{S1,d}$ is decreased to zero and the anti-parallel diode $D_{S1}$ is conducting. Therefore, the switch $S_1$ is turned on at this instant to achieve ZVS. Fig. 5 shows the measured gate voltage $v_{S2,g}$, the drain voltage $v_{S2,d}$ and the switch current $i_{S2}$ of the switch $S_2$ at 30%, 60% and 100% load conditions, respectively. Similarly, $S_2$ is also turned on at ZVS.

Fig. 6 shows the primary winding currents $i_{Lr1}$ and $i_{Lr2}$ and the switch currents $i_{S1}$ and $i_{S2}$ at 60% and 100% load conditions. When $S_1$ is in the on state, the switch current $i_{S2}$ is zero, the inductor current $i_{Lr1}$ increases and the inductor current $i_{Lr2}$ decreases and the switch current $i_{S1}=i_{Lr1}-i_{Lr2}$ at 60% and 100% load conditions. When $S_1$ is in the off state and $S_2$ is in the on state, the switch current $i_{S1}$ is zero. The inductor current $i_{Lr1}$ decreases, the inductor current $i_{Lr2}$ increases, and the switch current $i_{S2}=i_{Lr2}-i_{Lr1}$. Fig. 7 illustrates the measured results of the gate voltages $v_{S1,g}$ and $v_{S2,g}$, the clamp voltage $v_{Cc}$ and the capacitor voltage $v_C$ at 30%, 60% and 100% load conditions. It is clear that the clamp voltage $v_{Cc}$ is related to the duty cycle of the switch $S_1$. If the duty cycle $\delta$ is greater than 0.5, then $v_{Cc}$ is a negative voltage. On the other hand, $v_{Cc}$ is positive voltage if $\delta$ is less than 0.5.

Figs. 8 and 9 show the measured waveforms of the gate voltage $v_{S1,g}$, the secondary winding currents $i_{T1,s}$ and $i_{T2,s}$ and the diode currents $i_{D1,s}$-$i_{D4,s}$ at 60% and 100% load conditions. When $S_1$ is in the on state, the secondary winding current $i_{T1,s}$ is positive and the secondary winding current $i_{T2,s}$ is negative. Thus the diodes $D_1$ and $D_3$ are conducting. When $S_1$ is in the off state, the secondary winding current $i_{T1,s}$ is negative and the secondary winding current $i_{T2,s}$ is positive. Thus the diodes $D_2$ and $D_4$ are conducting. Fig. 10 gives the measured waveforms of gate voltage $v_{S1,g}$ and the output capacitor voltages $V_{o1}$ and $V_{o2}$ at 60% and 100% load conditions. It is clear that the capacitor voltages $V_{o1}$ and $V_{o2}$ are related to the duty cycle of the switch $S_1$. Fig. 11 shows the
Analysis and Implementation of a DC-DC Converter with an Active Snubber

Fig. 8. Measured waveforms of gate voltage $v_{S1,gs}$ and the secondary side currents of $T_1$ at (a) 60% load (b) 100% load.

Fig. 9. Measured waveforms of gate voltage $v_{S1,gs}$ and the secondary side currents of $T_2$ at (a) 60% load (b) 100% load.

Fig. 10. Measured waveforms of gate voltage $v_{S1,gs}$ and output capacitor voltages $V_{o1}$ and $V_{o2}$ at (a) 30% load (b) 100% load.

Fig. 11. Measured efficiencies of the proposed converter at different load conditions.

VI. CONCLUSION

In this paper, a parallel soft-switching converter with an output voltage doubler is proposed. An active snubber is adopted to realize the transformer flux reset, to limit the peak voltage on the semiconductors, and to achieve ZVS turn-on for the main and auxiliary switches. Thus the converter efficiency is increased. The two circuit modules are connected in parallel with the same switches to achieve load current sharing. A circuit analysis and a design example of the proposed circuit are discussed and presented in detail. Finally, experiments measured efficiencies of the proposed converter for different load conditions. The maximum efficiency of the proposed converter is 89.3% at 90% of full load. If the lower turn-on resistance of the MOSFETs is available and the skin effect of transformer winding is considered in the design of the circuit, the circuit efficiency of the adopted converter can be increased by about 3%-5%.
based on a 340W laboratory prototype have been provided to verify the theoretical analysis and the performance of the proposed converter.

REFERENCES


**Bor-Ren Lin** received his B.S. in Electronic Engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1988, and his M.S. and Ph.D. in Electrical Engineering from the University of Missouri, USA, in 1990 and 1993, respectively. From 1991 to 1993, he was a Research Assistant with the Power Electronic Research Center, University of Missouri. Since 1993, he has been with the Department of Electrical Engineering, National Yunlin University of Science and Technology, Douliou, Taiwan, where he is currently a Professor. He has authored more than 300 published technical conference and journal papers in the area of power electronics. His main research interests include power-factor correction, multilevel converters, active power filters, and soft-switching converters. Dr. Lin is an Associate Editor of the IEEE Transactions on Industrial Electronics and The Institution of Engineering and Technology Proceedings—Power Electronics. He was the recipient of Research Excellence Awards in 2004, 2005, and 2007 from the College of Engineering, National Yunlin University of Science and Technology. He received best paper awards from the IEEE Conference on Industrial Electronics and Applications 2007 and 2011, from the Taiwan Power Electronics 2007 Conference, and from the IEEE Power Electronics and Drive Systems 2009 Conference.

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