High Step-Down Multiple-Output LED Driver with the Current Auto-Balance Characteristic

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Abstract

A high step-down multiple-output LED driver is proposed in this paper. Firstly, the derivation of the driver with dual-output is presented and its operation principle and steady state performance are analyzed in detail. Secondly, a high step-down N-channel LED driver is proposed and its current auto-balance characteristic and step-down ratio are analyzed. Finally, an experimental prototype is built and the experimental results are given. The theoretical analysis and experimental results show that the proposed driver has the following virtues: First, if load balancing is achieved, the voltage gain is 1/N that of a Buck driver, where N is the number of channels. Second, each output automatically has an equal output current, without requiring more current close-loop control circuits than a Buck driver. Last, the voltage stresses of the switches and diodes are lower than those of a Buck driver, meaning that lower voltage switches and diodes can be used, and a higher efficiency can be expected.

Key words: DF buck, One cycle controller, Small signal model

I. INTRODUCTION

Due to the enormous progress recently achieved in solid-state lighting technology and its potential virtues of high efficiency, environmental friendliness, long lifetime, small size, etc, LEDs have been regarded as a promising technology to replace the energy-inefficient incandescent lamps and mercury-based fluorescent lamps [1]-[4]. LED drivers occupy an important place in the whole LED lighting system, and they have become a research hotspot in the field of power electronics [5]-[16]. When a LED driver utilize an ac voltage source as its input, the “classical” two-stage structure shown in Fig.1 is always adopted. This two-stage structure is composed of a PFC pre-regulator and a current regulator. The PFC pre-regulator is needed to convert the AC voltage to a regulated DC voltage. A high power factor and low-input-current harmonics are becoming mandatory design criteria. The current regulator is needed to drive LEDs with a constant current regardless of the number of LEDs. In this paper, the research focuses on the topology of the current regulator.

Although some of the trends in commercial LEDs are towards high power, high current devices, a large number of LEDs arranged in series, in parallel, or in a series and parallel combination are adopted in high power applications [14]-[16]. As the brightness of LEDs is directly related to their current, it is an effective way to ensure that each LED produces a similar light output by connecting all of the LEDs in series. However, the reliability of this arrangement is limited because the whole string of LEDs fails if one of them is damaged. On the other hand, the simple paralleling of LEDs is not desirable due to the current sharing related to both the LED’s exponential voltage-current characteristic and the negative temperature coefficient of the LED’s forward voltage drop [17]. There are several methods for driving multiple strings connected in parallel. A straightforward approach is to employ a current regulator for each string, where the current regulator can be of the linear or switch-mode type. Employing linear regulators suffers from poor operating efficiency. Employing a more efficient switch-mode regulator to drive each LED string can overcome the drawback of linear regulators. However, they have a higher component count and cost. As a result, a switch-mode current regulator with multi-outputs may be a
The output voltage of the PFC pre-regulator is always around 400V for a 220V AC system, while the voltage across the LED string is always below 40V limited by its cumulative voltage drop and reliability consideration. This means that the step-down ratio of the current regulator is above 10. How to realize this high step-down current regulator with high performance is an issue that must be solved. Theoretically, if the duty cycle D is close to zero, the step-down ratio of a Buck converter is extremely small. However, there are some limitations related to the Buck converters in high step-down conversion: 1) the voltage stress and current stress of the switches and diodes are quite large, which makes a low-voltage high-performance devices unsuitable; 2) the switching loss is large, which results in low efficiency; 3) the electromagnetic interference (EMI) noise is serious; 4) the transient response is limited by the small turn-on interval of the switches. To avoid an extremely small duty cycle, isolated type DC/DC converters may be employed, such as Flyback converter, Forward converter, Half-bridge converter, Full-bridge converter, etc. However, these isolated topologies are complicated when compared with a Buck converter. In addition, the leakage inductor of the transformer always results in large voltage stress and severe EMI. A center-tapped Buck converter maybe a good choice because of its simple topology [18]. However, because the leakage inductor of the center-tapped inductor always exits, the potential problem described above is unavoidable. Active clamp circuits can recover the leakage energy effectively and reduce the voltage stress of the switches [19]-[21]. However, the topology is then further complicated and additional losses related to these active clamp circuit exists. In [22], a LED driver circuit with series-input-connected converter cells was proposed. Since all of the converter cells are driven by the same duty cycle, the input voltage for each of the cells is balanced and the output currents are identical. Furthermore, the voltage stresses are lowered and low-voltage high-performance devices are used so high efficiency can be expected. However, it is impossible to turn on and turn off these switches at the exact same time, which leads to unevenness of the voltage stress. Therefore, the reliability is reduced. Additionally, the interactive influence among these converter cells makes it difficult to design the loop compensator.

In this paper, a high step-down multiple-output LED driver is proposed. This driver has the following potential virtues: 1) if the loads for each output are equal, namely, the number of LEDs for each string is the same, the voltage gain is 1/N that of a Buck driver, where N means the number of the output channels, thus avoiding an extremely small duty cycle; 2) the currents for each of the outputs are shared automatically if the duty cycle is the same, thus only one current close-loop control circuit is needed, and the current auto-balance characteristic is not affected by the number of LEDs per string; 3) the voltage stress of the switches is lower than that of Buck drivers, thus low voltage switches are suitable and high efficiency is expected.

This paper is organized as follows. The derivation of the high step-down two-output driver is presented in Section II. In section III, the operation principle of the proposed two-output driver is illustrated. A steady state performance analysis is presented in Section IV. In Section V, the high step-down N-channel driver is given and analyzed. Experimental results with a 30W 400V-input three-channel prototype are given in Section VI. Section VII summarizes the conclusions drawn from the investigation.

II. TOPOLOGY DERIVATION

The topology of buck driver is shown in Fig.2. Assume that the normal voltage across each of the LEDs is ULED and that the number of the series connected LEDs is m1. Therefore, the output voltage is denoted as m1ULED. When operating in continuous conduction mode and in the steady state, the step-down ratio (M1) can be represented as:

$$M_1 = \frac{m_1U_{LED}}{U_{in}} = D$$  \hspace{1cm} (1)

where D is the duty cycle.

In order to realize the high step-down ratio, a controllable voltage source can be inserted, as shown in Fig.3. According to the voltage-second balance requirement of inductor L1, its step-down ratio can be derived as:

$$M_1 = \frac{m_1U_{LED}}{U_{in}} = \left(1 - \frac{U_{cl}}{U_{in}}\right)D$$  \hspace{1cm} (2)

From (2), a higher step-down ratio than the Buck driver is realized provided that Ucl is greater than zero and smaller than...
It is well known that a capacitor can be treated as a voltage source provided that the ripple of the voltage across the capacitor can be neglected when compared with its dc value. Nonetheless, if the controllable voltage source is substituted directly by a capacitor, $C_1$, as shown in Fig.4, the converter can not operate in the steady state because it is impossible to satisfy the ampere-second balance requirement of capacitor $C_1$ during one switching period $T_s$. Then the voltage across the capacitor ($U_{c1}$) becomes higher and higher until eventually, the driver is damaged.

According to Fig.4, when switch $S_1$ is OFF and diode $D_1$ is kept ON, capacitor $C_1$ can be treated as the input voltage source of another buck converter, as shown in Fig.5. When switch $S_1$ is ON and $S_2$ is OFF, capacitor $C_1$ is charged. When switch $S_1$ is OFF and $S_2$ is ON, capacitor $C_1$ is discharged. Therefore, it is possible to satisfy the ampere-second balance requirement of $C_1$ in one switching period $T_s$. In the following section, the operating principle of the driver, shown in Fig.5, will be analyzed in detail.

III. OPERATING PRINCIPLE

To simplify the analysis, the following assumptions are made:

1) The switching-frequency current ripples of $i_{L1}$ and $i_{L2}$ are much smaller than their dc values, $I_{L1}$ and $I_{L2}$ respectively.

2) All of the components are ideal, and all of the parasitic parameters are neglected.

3) The driving signals of $S_1$ and $S_2$ are interleaved with a $180^\circ$ phase shift and their duty cycle $D$ is smaller than 0.5.

The key waveforms of the proposed driver are shown in Fig.6. There are four stages in one switching period. The corresponding equivalent circuits for each stage are shown in Fig.7.

**Stage 1** ($t_0 < t < t_1$ see Fig. 7(a)): This stage starts by turning switch $S_1$ on. As a result, diode $D_1$ is reverse-biased. Switch $S_2$ is OFF and diode $D_2$ conducts current $i_{L2}$. The voltage across $L_1$, $u_{L1}$, is equal to $U_{in}-U_{c1}-m_1U_{LED}$, which makes $i_{L1}$ linearly increase at a slope of $(U_{in}-U_{c1}-m_1U_{LED})/L_1$. As diode $D_2$ is in the conduction state, inductor $L_2$ bears a voltage of $m_2U_{LED}$, and the falling rate of $i_{L2}$ is $m_2U_{LED}/L_2$. In this stage, capacitor $C_1$ is charged by $i_{L1}$.

**Stage 2** ($t_1 < t < t_2$ see Fig. 7(b)): Switch $S_1$ is gated off at $t_1$, diode $D_1$ conducts to carry current $i_{L1}$, switch $S_2$ is OFF and diode $D_2$ is ON as in the former stage. During this interval, inductors $L_1$ and $L_2$ are discharged by $m_1U_{LED}$ and $m_2U_{LED}$ respectively. Current $i_{L1}$ decreases from its maximum value at a slope of $m_1U_{LED}/L_1$, and current $i_{L2}$ decreases to its minimum value at a slope of $m_2U_{LED}/L_2$. The current through capacitor $C_1$, $i_{L1}$, is zero and $U_{c1}$ is kept constant throughout this stage.

**Stage 3** ($t_2 < t < t_3$ see Fig. 7(c)): At time $t_2$, switch $S_2$ is gated ON and diode $D_1$ is blocked. Switch $S_1$ is kept OFF and diode $D_1$ is ON throughout the whole stage. Current $i_{L1}$ increases from its minimum value to its maximum value linearly with a slope of $(U_{in}-m_1U_{LED})/L_1$, and capacitor $C_1$ is discharged by $i_{L1}$ during this interval. Current $i_{L2}$ continue to decrease with a slope of $m_1U_{LED}/L_1$ in this stage. This interval ends when $S_2$ turns off at $t_3$.

**Stage 4** ($t_3 < t < t_4$ see Fig. 7(b)): The equivalent circuit of this stage is same as stage 2. Switches $S_1$ and $S_2$ are OFF and diodes $D_1$ and $D_2$ are ON. Current $i_{L1}$ decreases linearly to its
minimum value at time $t_4$ and current $i_{l_2}$ begins to decrease at time $t_3$. The decreasing rates of $i_{l_1}$ and $i_{l_2}$ are $m_1 \frac{U_{LED}}{L_1}$ and $m_2 \frac{U_{LED}}{L_2}$ respectively. This is the end of the switching cycle.

IV. STEADY PERFORMANCE ANALYSIS

A. Current Auto-balance Characteristic

In one switching period, capacitor $C_1$ is charged by current $i_{l_1}$ when switch $S_1$ is ON and switch $S_2$ is OFF. The charging time is $DT_s$. When $S_1$ is gated OFF and $S_2$ is turned ON, capacitor $C_1$ is discharged by current $i_{l_2}$ and the discharging time is also $DT_s$ because the driving signals of $S_1$ and $S_2$ are interleaved with the same duty cycle $D$. In steady state operation, the switching frequency ripples of $i_{l_1}$ and $i_{l_2}$ are ignored and their dc values are assumed to be $I_{l_1}$ and $I_{l_2}$, respectively. According to the ampere-second balance requirement of capacitor $C_1$, the following equation can be deduced:

$$DT_s I_{l_1} = DT_s I_{l_2}$$

$$I_{l_1} = I_{l_2}$$

From (3) or (4), only one current close-loop control circuit is needed to keep the two output currents equal. In other words, if current $I_{l_2}$ is controlled to be the nominal current of the LED, $I_{LED}$, current $I_{l_2}$ will automatically be $I_{LED}$.

B. Step-down Ratio

Applying the voltage-second balance requirement on $L_1$ and $L_2$, the following equations are deduced:

$$D(U_{in} - U_{C_1} - m_1 U_{LED}) = (1 - D) m_1 U_{LED}$$

$$D(U_{C_1} - m_2 U_{LED}) = (1 - D) m_2 U_{LED}$$

Assume that the step-down ratios of the first and second output are $M_1$ and $M_2$ respectively, the ratio of the capacitor voltage $U_c$ and the input voltage $U_{in}$ is $M_{c_1}$, namely:

$$M_1 = \frac{m_1 U_{LED}}{U_{in}}$$

$$M_2 = \frac{m_2 U_{LED}}{U_{in}}$$

$$M_{c_1} = \frac{U_{C_1}}{U_{in}}$$

From (5) to (9), the following equations are deduced:

$$M_1 + M_2 = D$$

$$M_{c_1} = \frac{M_2}{D}$$

When the number of LEDs for each string is the same, namely, $m_1 = m_2$, the following equations are deduced:

$$M_1 = M_2 = \frac{D}{2}$$

$$M_{c_1} = \frac{1}{2}$$

From (12), the step-down ratio of the proposed driver is double that of the buck driver, which is applicable in the field of high step-down applications.

C. Voltage Stresses of the Switching Devices

The voltage stress of switch $S_1$, $U_{stress-S1}$, and the voltage stress of diode $D_1$, $U_{stress-D1}$, can be derived as:

$$U_{stress-S1} = U_{stress-D1} = U_{in} - U_{C_1}$$

The voltage stress of switch $S_2$, $U_{stress-S2}$, and the voltage stress of diode $D_2$, $U_{stress-D2}$, can be obtained as:

$$U_{stress-S2} = U_{in}$$

$$U_{stress-D2} = U_{C_1}$$

From (12) to (16), when $m_1$ and $m_2$ are equal, the voltage stresses of switch $S_1$, diodes $D_1$ and $D_2$ are half the input voltage $U_{in}$, which means that switches and diodes with a
lower nominal voltage can be selected and higher efficiency can be expected. However, the maximum voltage across switch \( S_2 \) is the input voltage \( U_{in} \) when \( S_1 \) is ON and \( S_2 \) is OFF.

D. Current Stresses of the Switching Devices

The current stress of switch \( S_1 \), \( I_{stress-S1} \), is equal to the maximum value of \( i_{l1} \). The current stresses of switch \( S_2 \) and diode \( D_2 \), which are denoted as \( I_{stress-S2} \) and \( I_{stress-D2} \) respectively, are equal to the maximum value of \( i_{l2} \). They are represented as follows:

\[
I_{stress-S1} = I_{LED} + \frac{m_1 U_{LED}}{2L_1} (1 - D) T_S
\]

\[
I_{stress-S2} = I_{stress-D2} = I_{LED} + \frac{m_2 U_{LED}}{2L_2} (1 - D) T_S
\]

where \( U_{LED} \) and \( I_{LED} \) are the nominal voltage and nominal current of the LED, respectively.

However, the current stress of diode \( D_1 \), \( I_{stress-D1} \), is not equal to the maximum value of \( i_{l1} \). In stage 3, described in section III, the current through diode \( D_1 \) is the sum of \( i_{l1} \) and \( il_2 \). Therefore, \( I_{stress-D1} \) is absolutely greater than \( I_{stress-S1} \). The detail derivation of \( I_{stress-D1} \) is given in the Appendix, and the expression is derived as (A3).

E. Voltage Ripple of \( U_{ci} \)

The charging or discharging charge in one switching period, \( Q_{ci} \), is represented as:

\[
Q_{ci} = I_{LED} DT_S
\]

Therefore, the peak-to-peak ripple of voltage \( U_{ci} \), denoted as \( \Delta U_{ci} \), is derived as:

\[
\Delta U_{ci} = \frac{I_{LED} DT_S}{C_i}
\]

V. HIGH STEP-DOWN N-CHANNEL DRIVER

Based on the method described in section II, a high step-down \( N \)-channel driver is derived, as shown in Fig.8. The output current auto-balance and the high step-down ratio characteristics are analyzed in this section based on assumptions similar to those described in section III. It is worth noting that the driving signals of \( S_1, S_2, ..., S_N \), are interleaved with a \( 360^\circ/N \) phase shift and the duty cycle \( D_1 \) is smaller than \( 1/N \).

A. Current Auto-balance Characteristic

Applying the ampere-second balance requirement on \( C_1 \),

\[
\int_{0}^{T_S} i_{l1} dt = \int_{0}^{T_S} (I_{LED} + m_1 U_{LED}) dt
\]

\[
\frac{m_1 U_{LED}}{2L_1} (1 - D) T_S = I_{LED} DT_S
\]

\[
D(U_{in} - U_{c1} - m_1 U_{LED}) = (1 - D) m_1 U_{LED}
\]

Similarly, according to the voltage-second balance requirement of \( L_1 \), the following equation is deduced:

\[
D(U_{in} - U_{c1} - m_1 U_{LED}) = (1 - D) m_1 U_{LED}
\]

Finally, according to the voltage-second balance requirement of \( L_n \):
Fig. 9. Step-down ratio extension.

Fig.10. Experimental prototype circuit

In (28) \( i \) may be equal to 1, 2, \ldots, \( N-1 \).

When the number of LEDs for each string is equal, the output voltages are equal and the step-down ratio \( M \) can be represented as:

\[
M = M_1 = \cdots = M_i = \cdots = M_n = \frac{D}{N} \quad (29)
\]

\[
N \leq \frac{U_{in}}{U_o} \quad (30)
\]

From (29), an extremely small duty cycle can be avoided by choosing \( N \) properly and the step-down ratio extension is shown in Fig.9. In addition, the channel is limited to (30).

VI. EXPERIMENTAL RESULTS

In order to confirm the feasibility of the proposed high step-down driver, an experimental prototype circuit, as shown in Fig.10, has been built. The input voltage \( U_{in} \) is 400V; the nominal current of LED \( I_{LED} \) is 350mA; the number of 1W LEDs per string is ten; the switching frequency \( f_s \) is 150kHz; \( L_1, L_2 \) and \( L_3 \) are 1.5mH, \( C_1, C_2 \) and \( C_3 \) are equal to 0.1\( \mu \)F; \( S_1, S_2 \) and \( S_3 \) are IRFP460; \( D_1, D_2 \) and \( D_3 \) are MUR1640, and the control chip is an ISL6558 from Intersil. The isolated driver for \( S_1, S_2 \) and \( S_3 \) is based on a high speed MOSFET gate drive optocoupler (FOD3180).

The experimental results are shown in Fig.11. The gate signals of switches \( S_1, S_2 \) and \( S_3 \) denoted as \( Q_1, Q_2 \) and \( Q_3 \), are shown in Fig. 11(a). They are interleaved with a 120° phase shift and the duty cycle \( D \) is around 0.3. Fig. 11(b) shows the waveforms of \( i_{l1}, i_{l2} \) and \( i_{l3} \). Their average values are exactly equal to 350mA only by sampling \( i_{l1} \) to realize the current close-loop control. The waveforms of the voltage across \( C_1 \) and \( C_2 \), denoted as \( U_{c1} \) and \( U_{c2} \), are shown in Fig. 11(c). Their dc values are approximately two thirds and one third of the input voltage \( U_{in} \) respectively as predicted by (28). Fig. 11(d) shows the voltage waveforms across \( S_1, S_2 \) and \( S_3 \), which are denoted as \( u_{ds1}, u_{ds2} \) and \( u_{ds3} \), respectively. It is clear that the voltage stress of switch \( S_1 \) is about one third of the input voltage \( U_{in} \). When \( S_1 \) is ON and \( S_2 \) is OFF, the voltage across \( S_1 \) reaches its maximum value, which is about two thirds of the input voltage. When \( S_2 \) is ON and \( S_3 \) is OFF, \( S_1 \) bears the maximum voltage of two thirds of the input voltage. The voltage waveforms on diodes \( D_1, D_2 \) and \( D_3 \), denoted as \( u_{d1}, u_{d2} \) and \( u_{d3} \) respectively, are given in Fig. 11(e). Their maximum value is about one third of the input voltage, which is in accordance with the theoretical analysis.

Fig. 11(f) shows the waveforms of \( i_{l1}, u_{ds1}, i_{l2} \) and \( u_{ds2} \) when the number of LEDs for the first output changes from ten to five. It is shown that \( i_{l2} \) is unchanged though the value of \( i_{l1} \) is not directly controlled by a current close-loop control circuit. The measured efficiency of the driver under different loads is shown in Fig.12. The highest efficiency is 87.5%.

VII. CONCLUSION

A high step-down multiple-output LED driver is introduced in this paper. The operation principle and steady state performance are analyzed and experimental results are given. They show the following potential virtues related to the proposed driver: 1) if the number of LEDs for each string is equal, the step-down ratio is \( 1/N \) that of the Buck driver, where \( N \) means the number of outputs, which is appreciated in the field of high step-down applications where higher efficiency is expected; 2) because of the ampere-second balance requirement of the capacitors, the currents for each of the outputs are identical automatically if the duty cycle is the same, thus only one current close-loop control circuit is needed; 3) the voltage stress of the switches is lower than that of the Buck driver, thus low voltage switches are suitable and higher efficiency is possible. Based on the above, the
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The proposed driver is suitable in the field of LED lighting applications.

Fig. 11. Experimental waveforms. (a) Q1, Q2, Q3. (b) i_{L1}, i_{L2} and i_{L3}. (c) U_{C1} and U_{C2}. (d) u_{d1}, u_{d2}, u_{d3}. (e) u_{d1}, u_{d2}, u_{d3}. (f) i_{L1}, u_{O1}, i_{L2}, u_{O2}.

Fig. 12. The measured efficiency at different loads.

APPENDIX DERIVATION OF $I_{\text{STRESS-D1}}$

Referring to Fig. 6, consider the moment that switch $S_1$ is gated ON as the starting point of the time period so that $t_0$ is assumed to be zero. Currents $i_{L1}$ and $i_{L2}$ during the following switching period can be derived by the following equations:

$$i_{L1} = \begin{cases} i_{\text{in}} - \frac{m_{\text{SS}}}{2L_s} (1-D)T_s & (0 < t < DT_1) \\ \frac{m_{\text{SS}}}{2L_s} & (DT_1 < t < T_s) \end{cases}$$

$$i_{L2} = \begin{cases} i_{\text{in}} - \frac{m_{\text{SS}}}{2L_s} (1-D)T_s & (0 < t < DT_2) \\ \frac{m_{\text{SS}}}{2L_s} & (DT_2 < t < T_s) \end{cases}$$

The current stress of diode $D_1$, $I_{\text{STRESS-D1}}$, can be derived by the following equation:
\[ I_{\text{max}} = \max \left\{ I_0 (DT) + I_1 \left( \frac{T_1}{2} \right) + I_2 \left( \frac{T_2}{2} \right), \right. \]
\[ \left. I_0 \left( \frac{1 + 2D}{2} T_1 \right) + I_1 \left( \frac{1 + 2D}{2} T_2 \right) \right\} \]

\[ I_{\text{max}} + \frac{m_{U_{\text{max}}} (1-D) T_1}{2k} \]
\[ 2I_{\text{max}} + \frac{m_{U_{\text{max}}} \left(1-D\right) T_1}{2k} \]

\[ \text{ACKNOWLEDGMENT} \]


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