Interleaved ZVS Resonant Converter with a Parallel-Series Connection

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Abstract

This paper presents an interleaved resonant converter with a parallel-series transformer connection in order to achieve ripple current reduction at the output capacitor, zero voltage turn-on for the active switches, zero current turn-off for the rectifier diodes, less voltage stress on the rectifier diodes, and less current stress on the transformer primary windings. The primary windings of the two transformers are connected in parallel in order to share the input current and to reduce the root-mean-square (rms) current on the primary windings. The secondary windings of the two transformers are connected in series in order to ensure that the transformer primary currents are balanced. A full-wave diode rectifier is used at the output side to clamp the voltage stress of the rectifier diode at the output voltage. Two circuit modules are operated with the interleaved PWM scheme so that the input and output ripple currents are reduced. Based on the resonant behavior, all of the active switches are turned on under zero voltage switching (ZVS), and the rectifier diodes are turned off under zero current switching (ZCS) if the operating switching frequency is less than the series resonant frequency. Finally, experiments with a 1kW prototype are described to verify the effectiveness of the proposed converter.

Key words: Interleaved PWM, LLC converter, VCO, ZCS, ZVS

I. INTRODUCTION

To mitigate the environmental pollution and climate changes resulting from fossil fuel based power generation, soft switching power converters have been proposed recently to meet the demand for high efficiency from organizations such as the Environment Protection Agency (EPA) and the Climate Saver Computing Initiative (CSCI). There are two different kinds of control schemes related to the switching frequency in soft switching converters. One is based on a constant switching frequency with a variable duty cycle, while the other is based on a constant duty cycle and a variable switching frequency. Power converters with constant switching frequency and zero voltage switching (ZVS) techniques, such as active clamped ZVS converters [1]-[5], asymmetric half-bridge converters [6]-[7] and phase-shift pulse-width modulation (PWM) converters [8]-[9], have been proposed for many years to reduce the switching losses of MOSFETs and to increase circuit efficiency. However, the ZVS effect of these techniques is limited to specific load conditions. Thus it is difficult to design optimal converters with wide load ranges. Power converters with a variable switching frequency and the ZVS technique such as resonant converters [10]-[15] have been proposed to achieve ZVS turn-on or zero current switching (ZCS) turn-off for active switches. In a conventional series resonant converter, the output voltage cannot be properly regulated under the no-load condition due to its limited voltage gain. In order to overcome the drawbacks of conventional series resonant converters, LLC series resonant converters [16]-[19] have been presented that have the advantages of a high conversion efficiency, a high power density and a high voltage gain. If the switching frequency is less than the series resonant frequency, the rectifier diodes at the secondary side can be turned off under ZCS to overcome the reverse recovery losses.

This paper presents an interleaved series resonant converter to achieve ZVS turn-on for all of the active switches, ZCS turn-off for the rectifier diodes, ripple current reduction at the output capacitor and load current sharing. Two converter modules connected in parallel are used in the proposed circuit to share the load current and to reduce the current stress of the active switches. The interleaved PWM scheme is adopted to control the two circuit modules so that
the ripple current at the output capacitor partially cancelled each other out. For each circuit module, a series resonant converter with two transformers and a full-wave diode rectifier is adopted to realize soft switching for all of the semiconductors. The input impedance of the resonant tank is related to the operating switching frequency. Thus the output voltage can be regulated by the variable switching frequency for different input voltages and load conditions. Since the input impedance of the resonant tank is operated at an inductive load, the active switches can be turned on under ZVS and the rectifier diodes can be turned off under ZCS if the switching frequency is less than the resonant frequency. Thus the switching losses of the power switches and the reverse recovery losses of the rectifier diodes can be reduced. Two transformers are used in each circuit module to reduce the size of the magnetic core and to lessen the current stress on the primary windings. The secondary windings of the two transformers are connected in series in order to balance the transformer primary currents and to share the input current. For high output voltage applications, a full-wave diode rectifier is used in the secondary side to clamp the voltage stress of the rectifier diodes at the output voltage level. Compared to the conventional DC/DC converters used in low input voltage and high output voltage applications such as push-pull converters and symmetric half-bridge converters, the proposed converter has better circuit efficiency with a smaller size magnetic core and soft switching. Finally, experiments conducted on a 1kW prototype to verify the effectiveness of the proposed converter are described.

II. CIRCUIT CONFIGURATION

The basic block of a renewable energy power conversion system is given in Fig. 1(a). The front stage is a DC/DC converter and the second stage is a DC/AC inverter. Generally the input of the front stage comes from a PV based or fuel cell based renewable energy source with a low voltage input. The output of the DC/DC converter is a high DC voltage. Then a single-phase or a three-phase inverter is used to generate AC sinusoidal voltage. The circuit configuration of the proposed DC/DC converter is given in Fig. 1(b). Since the duty cycle for each of the active switches is equal to 0.5, the variable frequency modulation is adopted to regulate the output voltage. There are two circuit modules connected in parallel to share the input and output currents. The two circuit modules are operated with the interleaved scheme so that the input and output currents are partially cancelled. Therefore, the input and output ripple currents are reduced. Since the adopted circuit is used for high input current applications, the two transformers are connected in parallel in each of the circuit modules to share the input current. The secondary windings of the two transformers are connected in series in order to balance the two primary currents. \( V_{in} \) and \( V_o \) are the input and output terminal voltages. The input voltage \( V_{in} \) maybe a fuel cell voltage or a PV voltage from a solar panel. The first circuit module includes \( Q_1, Q_2, C_{r1}, L_{r1}, T_1, T_2, D_1-D_4 \) and \( C_o \). The primary windings of \( T_1 \) and \( T_2 \) are connected in parallel to share the input inductor current \( i_{L1} \). The secondary windings of \( T_1 \) and \( T_2 \) are connected in series to balance the primary currents, \( i_{T1} \approx i_{T2} \approx i_{L1}/2 \). The resonant tank in the first circuit module includes \( C_{r1}, L_{r1}, L_{m1} \) and \( L_{m2} \). \( D_1-D_4 \) are the rectifier diodes. \( C_1 \) and \( C_2 \) are the output capacitances of \( Q_1 \) and \( Q_2 \), respectively. \( C_o \) is the output capacitance. Full-wave diode rectifiers are adopted in the secondary side in order to reduce the voltage stress on the rectifier diodes for high output voltage applications. The components of the second circuit module are \( Q_3, Q_4, C_{r2}, L_{r2}, T_3, T_4, D_5-D_8 \) and \( C_o \). The primary and secondary windings of \( T_3 \) and \( T_4 \) are connected in parallel and series respectively to share the input inductor current \( i_{L2} \) and to balance the two primary currents \( i_{T3} \approx i_{T4} \). The resonant tank in the second circuit module includes \( C_{r2}, L_{r2}, L_{m3} \) and \( L_{m4} \). Based on the series resonant phenomenon, the active switches \( Q_3-Q_4 \) are turned on under ZVS if the resonant tank is operated as an inductive load. Therefore, the switching losses on the active switches are reduced to increase the circuit efficiency. On the other hand, the rectifier diodes can be turned off under ZCS if the switching frequency of the proposed converter is less than the series resonant frequency under a full load and a maximum input voltage. Thus the reverse recovery losses on fast recovery diodes are reduced. The proposed converter can be used for low input voltage and high output voltage applications such as push-pull converter and the second stage is a DC/AC inverter.
applications such as the battery-based DC/DC converters, the high power discharger systems and the DC/DC converters used in renewable energy systems.

III. OPERATION PRINCIPLE AND SYSTEM ANALYSIS

Each switch in the proposed converter is turned on with a 50% duty ratio. Therefore the output voltage regulation is controlled by a frequency modulation technique. The components of the two circuit modules are identical. The four transformers have the same turns ratio \( n = n_p/n_s \) and the same magnetizing inductance \( L_m \). All of the active switches are ideal and have the same output capacitance \( C_i = C_s = C_i = C_i = C_{eq} \). Fig. 2 shows the key waveforms during a switching cycle. There are twelve operating modes in the proposed converter for each switching period. The equivalent circuits for each of the operating modes are shown in Fig. 3.

Before time \( t_o \), \( Q_3 \), \( D_2 \), \( D_3 \) and \( D_4 \) conduct. \( C_i \) is charged and \( C_s \) is discharged.

Mode 1 \( [t_o \leq t \leq t_1] \): At time \( t_o \), \( C_s \) is discharged to zero voltage. Since \( i_{Q2} > 0 \), the anti-parallel diode of \( Q_2 \) conducts. Switch \( Q_2 \) can be turned on at this moment to achieve ZVS. Since \( i_{T7} = i_{Lm1}, i_{T8} = i_{Lm2}, i_{T9} = i_{Lm3} \) and \( i_{T10} = i_{Lm4}, \) diodes \( D_2, D_3, D_4 \) and \( D_5 \) conduct in this mode so that \( v_{Lm1} = v_{Lm2} = nV_o/2 \) and \( v_{Lm3} = v_{Lm4} = nV_o/2 \). The magnetizing currents \( i_{Lm1} \) and \( i_{Lm2} \) decrease linearly with a slope of \(-nV_o/(2L_m)\) and the magnetizing currents \( i_{Lm3} \) and \( i_{Lm4} \) increase linearly with a slope of \( nV_o/(2L_m)\). \( C_s \) and \( L_s \) are resonant with the applied voltage \( nV_o/2 \) in circuit module 1, while \( C_s \) and \( L_s \) are resonant with the applied voltage \( V_o - nV_o/2 \) in circuit module 2. \( i_{Ls1} \) and \( v_{C3,s} \) decrease, and \( i_{Ls2} \) and \( v_{C3,ss} \) increase in this mode. The resonant inductor currents \( i_{Lm1} \) and \( i_{Lm2} \) and the capacitor voltages \( v_{C3,s} \) and \( v_{C3,ss} \) in this mode are expressed as:

\[
i_{Lm1}(t) = V_o - nV_o/2 - v_{Q3,s}(t_0) \sin \omega_r(t - t_o) + i_{Lm2}(t_0) \omega_r(t - t_o)
\]

\[
v_{C3,s}(t) = V_o - nV_o/2 - v_{Q3,s}(t_0) \cos \omega_r(t - t_o) + i_{Lm2}(t_0) \omega_r(t - t_o)
\]

\[
i_{Lm2}(t) = V_o - nV_o/2 - v_{Q3,ss}(t_0) \sin \omega_r(t - t_o) + i_{Lm2}(t_0) \omega_r(t - t_o)
\]

\[
v_{C3,ss}(t) = V_o - nV_o/2 - v_{Q3,ss}(t_0) \cos \omega_r(t - t_o) + i_{Lm2}(t_0) \omega_r(t - t_o)
\]

where \( \omega_r = 1/\sqrt{L_sC_s} \). Power is transferred from the input terminal voltage \( V_o \) to the output load through \( Q_3, C_s, L_s, T_1, T_2, D_3 \) and \( D_4 \). This mode ends at time \( t_1 \) when \( i_{Lm1} = i_{Lm2} \) and \( i_{Lm3} = i_{Lm4} \). Then diodes \( D_3 \) and \( D_5 \) are off.

Mode 2 \( [t_1 \leq t \leq t_2] \): This mode starts at \( t_1 \) when \( i_{Lm1} = i_{Lm2} \) and \( i_{Lm3} = i_{Lm4} \). Then diodes \( D_3 \) and \( D_5 \) are off in circuit module 2. Since \( Q_3 \) still conducts in this mode, \( C_i, L_{r2}, L_{r3} \) and \( L_{r4} \) are resonant in circuit module 2. On the other hand, \( C_s, L_{r4} \) and \( L_{r4} \) are also resonant with the input voltage \( V_o/2 \). \( i_{Ls2} \) and \( v_{C3,ss} \) are obtained as:

\[
i_{Lm2}(t) = V_o - nV_o/2 - v_{Q3,ss}(t_0) \sin \omega_r(t - t_1) + i_{Lm2}(t_1) \cos \omega_r(t - t_1)
\]

\[
v_{C3,ss}(t) = V_o - nV_o/2 - v_{Q3,ss}(t_0) \cos \omega_r(t - t_1) + i_{Lm2}(t_1) \omega_r(t - t_1)
\]

where \( Z_p = \sqrt{L_s/L_c} \) and \( \omega_r = 1/\sqrt{(L_s + L_m/2)C_s} \).

The operation of circuit module 1 in this mode is the same as the operation in mode 1.

Mode 3 \( [t_2 \leq t \leq t_3] \): At time \( t_2 \), \( Q_3 \) is turned off and diodes \( D_5 \) and \( D_3 \) conduct. Thus \( v_{Lm1} = V_o/2 \) and \( v_{Lm2} = V_o/2 \) and \( i_{Lm3} \) and \( i_{Lm4} \) decrease in this mode. Since \( i_{Lm1} = 0 \), \( C_s \) is charged and \( C_s \) is discharged. If the energy stored in \( L_{r3} \) at time \( t_2 \) is greater than the energy stored in \( C_s \) and \( C_i \), then \( C_s \) can be discharged to zero voltage at time \( t_3 \). The capacitor voltages \( v_{C3} \) and \( v_{C4} \) are expressed as:

\[
v_{C3}(t) = v_{Lm1}(t_2)(t - t_2)/(2C_{eq})
\]

\[
v_{C4}(t) = V_o - i_{Lm2}(t_2)(t - t_2)/(2C_{eq})
\]

The operation behavior of circuit module 1 is the same as the circuit operation in mode 2.

Mode 4 \( [t_3 \leq t \leq t_4] \): At time \( t_3 \), \( C_s \) is discharged to zero voltage so that the anti-parallel diode of \( Q_4 \) conducts. Before \( i_{Q4} \) becomes positive, \( Q_4 \) is turned on under ZVS. Since \( D_2, D_3, \)
$D_6$ and $D_7$ conduct in this mode, the magnetizing voltages $v_{Lm1}=v_{Lm2}=v_{Lm3}=-nV_o/2$. Thus $i_{Lm1}$ and $i_{Lm2}$ decrease in this mode. $C_{1z}$ and $L_{1z}$ are resonant in circuit module 1, while $C_{2z}$ and $L_{2z}$ are resonant in circuit module 2.

Mode 5 ($t_5 \leq t_5 < t_6$): At time $t_5$, $i_{Lm3}=i_{T1}$ and $i_{Lm4}=i_{T2}$ in circuit module 1 such that diodes $D_7$-$D_9$ are reverse biased. Since $Q_2$ still conducts, $C_{1z}$, $L_{1z}$, $L_{2z}$ and $L_{4z}$ are resonant in this mode. The operation behavior of circuit module 2 is the same as the circuit operation in mode 4.

Mode 6 ($t_5 \leq t_5 < t_6$): At time $t_5$, $Q_3$ turns off and diodes $D_1$ and $D_3$ conduct so that $v_{Lm1}=v_{Lm2}=nV_o/2$. Therefore, $i_{Lm1}$ and $i_{Lm2}$ increase in this mode. Since $i_{Lm1}(t_5)<0$, $C_{1z}$ is discharged and $C_{2z}$ is charged. If the energy stored in $L_{1z}$ at time $t_5$ is greater than the energy stored in $C_{1z}$ and $C_{2z}$, then $C_1$ can be discharged to zero voltage at time $t_6$. The operation behavior of circuit module 2 in this mode is the same as the operation in mode 5.

Mode 7 ($t_5 \leq t_5 < t_6$): At time $t_6$, $C_1$ is discharged to zero voltage. Since $i_{Q1}<0$, the anti-parallel diode of $Q_1$ conducts. Therefore, $Q_1$ can be turned on at this moment to achieve ZVS. Since $D_1$, $D_5$, $D_7$ and $D_9$ conduct in this mode, $v_{Lm1}=v_{Lm2}=nV_o/2$ and $v_{Lm1}=v_{Lm2}=-nV_o/2$ so that $i_{Lm1}$ and $i_{Lm2}$ increase, while $i_{Lm3}$ and $i_{Lm4}$ decrease. $L_{1z}$ and $C_{1z}$ are resonant with the applied voltage $V_o-nV_o/2$ in circuit module 1, while $L_{2z}$ and $C_{2z}$ are resonant with the applied voltage $nV_o/2$ in circuit module 2.

Mode 8 ($t_6 \leq t_6 < t_7$): At time $t_7$, $i_{Lm1}=i_{T3}$ and $i_{Lm4}=i_{T4}$ so that diodes $D_3$-$D_4$ are off. Since $Q_4$ still conducts, $C_{1z}$, $L_{1z}$, $L_{2z}$ and $L_{4z}$ are resonant in module 2. The circuit operation of circuit module 1 is the same as the circuit operation in mode 7.

Mode 9 ($t_7 \leq t_7 < t_8$): At time $t_8$, $Q_4$ is turned off and diodes $D_3$ and $D_5$ conduct. Therefore, $v_{Lm3}=v_{Lm4}=nV_o/2$ and the magnetizing currents $i_{Lm3}$ and $i_{Lm4}$ increase in this mode. Since $i_{Lm3}(t_7)<0$, $C_3$ is charged and $C_4$ is discharged. If the energy stored in $L_{2z}$ at time $t_8$ is greater than the energy stored in $C_3$ and $C_4$, then $C_1$ can be discharged to zero voltage at time $t_9$. The operation behavior of circuit module 1 in this mode is the same as the circuit operation in mode 8.
Fig. 3 Operation modes of the proposed converter during one switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8 (i) mode 9 (j) mode 10 (k) mode 11 (l) mode 12.

Fig. 4. Equivalent circuit of circuit module 1.
Mode 10 \([t_9 \leq t < t_{10}]:\) At time \(t_9,\) capacitor \(C_3\) is discharged to zero voltage. Since \(i_{Lm1}(t_9) < 0,\) the anti-parallel diode of \(Q_1\) conducts. Thus \(Q_2\) can be turned on at this moment to achieve ZVS. Diodes \(D_1, D_4, D_3\) and \(D_5\) conduct in this mode so that \(v_{Lm1}=v_{Lm2}=v_{Lm3}=-nV_s/2.\) The magnetizing currents \(i_{Lm1} \approx i_{Lm2}\) increase in this mode. Input power is delivered to the output load through \(Q_1, C_{r1}, L_{r1}, T_1, T_2, D_1\) and \(D_2\) in circuit module 1 and through \(Q_2, C_{r2}, L_{r2}, T_3, T_4, D_3\) and \(D_4\) in circuit module 2. Therefore, \(i_{Lm1}, i_{Lm2}, v_{C2}f\) and \(v_{C2}f\) increase.

Mode 11 \([t_{10} \leq t < t_{11}]:\) At time \(t_{10},\) \(i_{Lm1}=i_{T2}\) and \(i_{Lm2}=i_{T2}\) so that diodes \(D_5-D_4\) are all off in circuit module 1. Since \(Q_1\) still conducts, \(C_{r1}, L_{r1}, L_{m1}\) and \(L_{m2}\) are resonant with the applied voltage \(V_{in}.\) The operation behavior of circuit module 2 in this mode is the same as the circuit operation in mode 10.

Mode 12 \([t_{11} \leq t < T_{t9}):\) At time \(t_{11}, Q_2\) is turned off and diodes \(D_2\) and \(D_3\) conduct. Thus \(v_{Lm1}=v_{Lm2}=-nV_s/2.\) The magnetizing currents \(i_{Lm1}\) and \(i_{Lm2}\) decrease in this mode. Since \(i_{Lm1}(t_{11})>0,\) \(C_1\) is charged and \(C_3\) is discharged. If the energy stored in \(L_{r1}\) at time \(t_{11}\) is greater than the energy stored in \(C_1\) and \(C_2,\) then \(C_2\) can be discharged to zero voltage at time \(T_{t9} .\) Then the anti-parallel diode of \(Q_2\) conducts. This is the last operating mode of the proposed converter during one switching period.

The power flow through the resonant tank is related to the switching frequency. All of the harmonics of the switching frequency are neglected in the following analysis. Fig. 4 shows an equivalent circuit of circuit module 1. The duty ratios of switches \(Q_1\) and \(Q_2\) are equal to 0.5. The input voltage of the resonant tank is a square waveform between 0 and \(V_{in}.\) The DC value and the fundamental root-mean-square (rms) value of the input voltage \(v_{C2}\) are \(V_{in}/2\) and \(\sqrt{2}V_{in}/\pi,\) respectively. The output side of circuit module 1 is driven by a quasi-sinusoidal current. When inductor current \(i_{T1}=i_{Lm1}, D_1\) and \(D_4\) conduct and \(v_{Lm1}=v_{Lm2}=nV_s/2.\) If \(i_{T1} \leq i_{Lm1},\) then \(D_3\) and \(D_1\) conduct and \(v_{Lm1}=v_{Lm2}=-nV_s/2.\) Thus the fundamental rms value of the magnetizing voltage is expressed as \(v_{Lm1,rms}=\sqrt{2}nV_s/\pi.\) Since the output current of circuit module 1 is equal to \(I_{L2},\) the rms value of the secondary winding current is equal to \(i_{L1,2,rms}=\pi I_{L2}/(4\sqrt{2}).\) Thus the load resistance \(R_o\) reflected to the transformer primary side is given as:

\[
R_{ac1} = R_{ac2} = \frac{v_{Lm1,rms}}{i_{L1,2,rms}/n} = \frac{8n^2}{\pi^2} R_o
\]

(9)

The AC resonant tank (\(L_{r1}\) and \(C_{r1}\)), shown in Fig. 5, is excited by an effectively sinusoidal input voltage \(v_{C2}f\) and it drives the effective resistive loads \(R_{ac1}\) and \(R_{ac2}\) in circuit module 1. The AC voltage gain of circuit module 1, based on Fig. 5, is expressed in (10).

![Fig. 5. AC resonant tank of circuit module 1 with fundamental switching frequency.](image-url)

**Table I**

**Key Circuit Parameters of the Prototype Circuit**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage (V_{in})</td>
<td>42 V–52 V</td>
</tr>
<tr>
<td>Output voltage (V_o) / Current (I_o)</td>
<td>400V/2.5 A</td>
</tr>
<tr>
<td>Series resonant frequency (f_s)</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Switches (Q_1-) (Q_2)</td>
<td>IRFP064</td>
</tr>
<tr>
<td>Diodes (D_1-) (D_4)</td>
<td>30ETH06</td>
</tr>
<tr>
<td>Turns ratio of (T_1-) (T_4)</td>
<td>(n_p/n_s=6:42)</td>
</tr>
<tr>
<td>Resonant inductances (L_{r1}, L_{r2})</td>
<td>0.633µH</td>
</tr>
<tr>
<td>Magnetizing inductances (L_{m1}, L_{m2})</td>
<td>7.6µH</td>
</tr>
<tr>
<td>Resonant capacitances (C_{r1}, C_{r2})</td>
<td>4µF</td>
</tr>
<tr>
<td>Output capacitor (C_o)</td>
<td>1320µF/450V</td>
</tr>
</tbody>
</table>

\[|G_{ac}(f)| = 1/\sqrt{\left[1 + k(1 - \frac{f_s^2}{f_o^2})\right]^2 + Q^2\left(\frac{f_s}{f_o} - \frac{f_s^2}{f_o^2}\right)^2} (10)\]

where \(f_s = 1/(2\pi\sqrt{L_{r1}/C_{r1}}),\) \(Q = \sqrt{L_{r1}/C_{r1}}/(R_{ac1}/2) ,\) \(k=2L_{r1}/L_{m1}\) and \(f_o,\) is the switching frequency. The AC voltage gain is related to the switching frequency in (10). Therefore, the output voltage \(V_o\) can be regulated by the variation of the switching frequency \(f_s.\) Under the no load condition, \(R_{ac1}\) is infinite and the quality factor \(Q\) equals zero. Then the AC voltage gain under the no load condition is expressed as:

\[|G_{ac}(f)|_{Q=0}=1/[1 + k(1 - \frac{f_s^2}{f_o^2})].\]

If the design minimum DC voltage gain at the maximum input voltage and the maximum switching frequency is greater than the AC voltage gain under the no load condition, then the output voltage \(V_o\) can be controlled.

\[G_{dc,min} = \frac{n(V_o + 2V_{tr})}{V_{in,\text{max}}} \geq 1/[1 + k(1 - \frac{f_s^2}{f_o^2})] (11)\]

where \(V_{tr}\) is the voltage drop across diodes \(D_1-\) \(D_4\) and \(f_{s,\text{max}}\) is the maximum switching frequency generated by the voltage controlled oscillator.

**IV. Experimental Results**
Experimental results based on a laboratory prototype have been provided to demonstrate the performance of the proposed converter. The circuit parameters of the prototype circuit are shown in Table I. The variable switching frequency is adopted to generate the gate signals. The flip-flop circuits are used to generate the interleaved PWM signals. First, an LLC control IC based on a L6599 is used to generate two PWM signals. Then, two D-type flip-flop ICs are used to generate four PWM signals. Fig. 6 gives the experimental results for the gate voltages of $Q_1$ to $Q_4$ at different input voltages and the full load condition. It can be observed that the gate voltage $v_{Q_3,gs}$ lags the gate voltage $v_{Q_1,gs}$ by one fourth of a switching period, and that the low input voltage $v_{Q_1,gs}$ $v_{Q_2,gs}$ $v_{Q_3,gs}$ $v_{Q_4,gs}$ $4\mu s$ (a) $v_{Q_1,gs}$ $v_{Q_2,gs}$ $v_{Q_3,gs}$ $v_{Q_4,gs}$ $4\mu s$ (b) $v_{Q_1,gs}$ $v_{Q_2,gs}$ $v_{Q_3,gs}$ $v_{Q_4,gs}$ $4\mu s$ (c) $v_{Q_1,gs}$ $v_{Q_2,gs}$ $v_{Q_3,gs}$ $v_{Q_4,gs}$ $4\mu s$ in the circuit. Fig. 6. results of gate voltages of $Q_1$ to $Q_4$ at full load and input voltage (a) $V_{in}=42V$ (b) $V_{in}=48V$ (c) $V_{in}=52V$ $[v_{Q_{1,gs}}]$-$v_{Q_{4,gs}}$:10V/div].

Fig. 7. Measured gate voltage and drain voltage at $V_{in}=48V$ and full load condition (a) $Q_1$ and $Q_2$ (b) $Q_3$ and $Q_4$ $[v_{Q_{1,gs}}]$-$v_{Q_{4,gs}}$:10V/div; $v_{Q_{1,ds}}$-$v_{Q_{4,ds}}$:50V/div].

Fig. 8. Measured results of gate voltages, $v_{Q_{1,gs}}$ and $v_{Q_{3,gs}}$, switch currents, $i_{Q1}$ and $i_{Q3}$, and the DC input current $i_{in}$ at $V_{in}=48V$ and full load condition $[v_{Q_{1,gs}}]$-$v_{Q_{3,gs}}$:10V/div; $i_{Q1}$, $i_{Q3}$, $i_{in}$:50A/div].

are used to generate four PWM signals. Fig. 6 gives the experimental results for the gate voltages of $Q_1$ to $Q_4$ at different input voltages and the full load condition. It can be observed that the gate voltage $v_{Q_3,gs}$ lags the gate voltage $v_{Q_1,gs}$ by one fourth of a switching period, and that the low input voltage $v_{Q_1,gs}$ $v_{Q_2,gs}$ $v_{Q_3,gs}$ $v_{Q_4,gs}$ $4\mu s$ in the circuit. Fig. 6. results of gate voltages of $Q_1$ to $Q_4$ at full load and input voltage (a) $V_{in}=42V$ (b) $V_{in}=48V$ (c) $V_{in}=52V$ $[v_{Q_{1,gs}}]$-$v_{Q_{4,gs}}$:10V/div].

Fig. 7. Measured gate voltage and drain voltage at $V_{in}=48V$ and full load condition (a) $Q_1$ and $Q_2$ (b) $Q_3$ and $Q_4$ $[v_{Q_{1,gs}}]$-$v_{Q_{4,gs}}$:10V/div; $v_{Q_{1,ds}}$-$v_{Q_{4,ds}}$:50V/div].

Fig. 8. Measured results of gate voltages, $v_{Q_{1,gs}}$ and $v_{Q_{3,gs}}$, switch currents, $i_{Q1}$ and $i_{Q3}$, and the DC input current $i_{in}$ at $V_{in}=48V$ and full load condition $[v_{Q_{1,gs}}]$-$v_{Q_{3,gs}}$:10V/div; $i_{Q1}$, $i_{Q3}$, $i_{in}$:50A/div].
voltage has less switching frequency. The measured gate voltage and the drain voltage of \( Q_1 \sim Q_4 \) at an input voltage of \( V_{in}=48V \) and the full load condition are given in Fig. 7. Before \( Q_1 \sim Q_4 \) are turned on, the drain voltages have been decreased to zero voltage. Therefore switches \( Q_1 \sim Q_4 \) are turned on under ZVS from 20% to 100% load conditions. Fig. 8 gives the measured waveforms of the gate voltages, \( v_{Q1,gs} \) and \( v_{Q3,gs} \), the switch currents, \( i_{Q1} \) and \( i_{Q3} \), and the DC input current \( i_{in} \) at \( V_{in}=48V \) and the full load condition. Since the currents \( i_{Q1} \) and \( i_{Q3} \) are phase-shifted by one-fourth of a switching period, the input current \( i_{in} \) has less current ripple.

Fig. 9 shows the measured resonant inductor currents, \( i_{Lr1} \) and \( i_{Lr2} \), and the resonant capacitor voltages, \( v_{Cr1} \) and \( v_{Cr2} \) at full load condition. Fig. 10 gives the measured waveforms of \( v_{Q1,gs} \), \( v_{Q3,gs} \), the switch currents, \( i_{Q1} \) and \( i_{Q3} \), and the DC input current \( i_{in} \) at \( V_{in}=48V \) and the full load condition. Since the currents \( i_{Q1} \) and \( i_{Q3} \) are phase-shifted by one-fourth of a switching period, the input current \( i_{in} \) has less current ripple.

Fig. 11 shows the measured waveforms of the gate voltages, \( v_{Q1,gs} \) and \( v_{Q3,gs} \), and the diode currents \( i_{D1} \), \( i_{D3} \), \( i_{D5} \) and \( i_{D7} \) at \( V_{in}=48V \) and full load condition. Before switches \( Q_1 \sim Q_4 \) are turned off, the rectifier diode currents are decreased to zero. Thus diodes \( D_1 \sim D_8 \) are all turned off under ZCS. Therefore, the reverse recovery losses of the rectifier diodes are reduced. Fig. 12 gives the measured results of the output currents \( i_{D1}+i_{D3} \) and \( i_{D5}+i_{D7} \) of the two circuit modules, the resultant output current \( i_{D1}+i_{D3}+i_{D5}+i_{D7} \) and the load voltage at the full load condition. The current \( i_{D1}+i_{D3} \) has less ripple current when compared to the ripple currents of \( i_{D5}+i_{D7} \) and \( i_{D3}+i_{D5} \). The measured switching frequencies with different input voltages and different load conditions are shown in Fig. 13. The high input voltage requires a low DC voltage gain. Therefore, the operating switching frequency increases if the input terminal voltage \( V_{in} \) increases. A lower switching frequency is necessary if the load power is increased at the constant input terminal voltage. The measured efficiencies of the proposed converter under different load conditions are given in Fig. 14.

Fig. 9. Measured resonant inductor currents, \( i_{Lr1} \) and \( i_{Lr2} \), and resonant capacitor voltages, \( v_{Cr1} \) and \( v_{Cr2} \) at full load condition [\( i_{Lr1}, i_{Lr2}: 50V/div; v_{Cr1}, v_{Cr2}: 50A/div \)].

Fig. 10. Measured waveforms at nominal input voltage and full load (a) \( v_{Q1,gs}, i_{Lr1}, i_{T1} \) and \( i_{T2} \) for converter module 1 (b) \( v_{Q3,gs}, v_{Q1,gs}: 10V/div; i_{Lr1}, i_{T1}, i_{T2}, i_{T3}, i_{T4}: 50A/div \).

Fig. 11. Measured waveforms of the gate voltages, \( v_{Q1,gs} \) and \( v_{Q3,gs} \), and diode currents \( i_{D1}, i_{D3}, i_{D5} \) and \( i_{D7} \) at \( V_{in}=48V \) and full load condition [\( v_{Q1,gs}, v_{Q3,gs}: 10V/div; i_{D1}, i_{D3}, i_{D5}, i_{D7}: 2A/div \)].
This paper presents an interleaved series resonant converter to achieve ZVS turn-on for active switches and ZCS turn-off for rectifier diodes. Thus the switching losses and the reverse recovery losses of the power semiconductors are reduced and the ripple current at the output capacitor is also reduced. In each circuit module, two transformers are used to reduce the power rating of each magnetic core. The primary windings of the two transformers are connected in parallel and the secondary windings are connected in series in order to reduce and balance the current rating on each transformer. Thus the small size of the magnetic cores and reduced winding turns are adopted in each transformer. A full-wave diode rectifier is used in the high voltage side to clamp the voltage stress of the diodes at the output terminal voltage instead of at two times the output voltage as in a conventional center-tapped rectifier. The proposed converter can be used for low input voltage and high output voltage applications such as battery stack power conversion systems and renewable energy conversion systems. Finally experimental results are provided to verify the performance of the proposed converter.

ACKNOWLEDGMENT

The project is supported by the National Science Council of Taiwan, ROC, under Grant NSC101-2221-E-224-MY2.

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Interleaved ZVS Resonant Converter with a Parallel-Series Connection

[537]

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