Integrated DC-DC Converter Based Energy Recovery Sustainer Circuit for AC-PDP

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Abstract

A new sustainer with primary-side integration of DC/DC converters and energy recovery circuits is proposed. The proposed circuit operates as a DC-DC converter during address period and energy recovery circuit during sustain period. Therefore, the conventional three electronic circuits composed of the power supply, X-driver, and Y-driver can be reduced to one circuit. As a result, it has desirable advantages such as a simple structure, less mass, fewer devices and cost reduction. Moreover, since the Zero Voltage Switching (ZVS) of all power switches can be guaranteed, a switching loss can be considerably decreased. To confirm the operation, validity, and features of the proposed circuit, experimental results from a prototype for 42-inch PDP are presented.

Keywords: ADS(Address Display-period Separation) method, Energy Recovery Circuit, Plasma Display Panel, Sustain driver

I. INTRODUCTION

As high-definition digital broadcasting era comes, the flat panel display market is fulfilled by the two main axes of the liquid crystal display (LCD) and plasma display panel (PDP) TV. The PDP has many advantages such as large screen size, self-luminous display, high contrast, and fast response compared with the LCD [1], [2]. However, due to the rapid progress of the large size LCD and LED TV, the PDP is losing competitiveness in flat panel display market. To overcome these kinds of situations, various researches and developments to minimize the cost have been done.

Fig. 1 shows the configuration of the conventional PDP driver. The conventional PDP driver is composed of a panel part and a driver part. The driver part is made up of electronic circuits such as a power supply, X driver, Y driver, logic board, and etc. To drive the PDP, the X and Y drivers require many kinds of power sources such as a sustain voltage \(V_s\), address voltage \(V_a\), and so forth. To generate these voltage sources, the LL-converter is usually used due to its desirable merits such as the high power conversion efficiency, low cost, and excellent dynamic characteristics.

Generally, the PDP needs a high-voltage and high-frequency switching power circuit called X and Y drivers to ignite the gas discharge of the PDP. The X and Y drivers have a full-bridge configuration to convert a DC high voltage to an AC high-voltage high-frequency square-wave pulses. Since the X and Y electrodes of the PDP are covered by the dielectric layer, the PDP is regarded as a capacitive load \(C_P\). Therefore, when we apply AC high-voltage high-frequency square-wave pulses with the amplitude of \(V_P\) between X and Y electrodes, the undesirable energy loss of \(2C_PV_P^2\) is generated during charging and discharging intervals without an energy recovery circuit. Moreover, the excessive surge charging and discharging currents will give rise to EMI noises and increase the surge current ratings of switches. To relieve these problems, several previous X and Y drivers called energy recovery circuits (ERCs) have been proposed [3]-[8].
Among hitherto developed ERCs, the Weber and Wood energy recovery circuit shown in Fig. 2 is most frequently used thanks to the high efficiency and good circuit flexibility [5], [9], [10]. Although it can recover most of the lost energy, it still has several drawbacks. Its two identical large auxiliary ERCs on both sides of the PDP are composed of four active power switches, eight power diodes, two inductors and two external capacitors. Also the conventional PDP system consists of cascaded two power stages that are the DC/DC power stage and the driving stage. Therefore, the conventional PDP system has several disadvantages such as its bulky size, poor efficiency, and high production cost. The sustain drivers proposed in [4], [5] and [6] reduce two switches and several diodes. Although they can achieve cost-effective sustain driver, they still have bulky inductors and several external capacitors. Therefore, the peak values and r.m.s. values of the inductor currents are high [6]. A sustain driver using the voltage stress reduction technique is proposed in [7]. Its circuit reduces two clamp diodes and voltage stress of the main switches by half, i.e., $V_s$, compared with a conventional single sustain driver. However, the voltage stress of the auxiliary switches is same as the conventional sustain driver. The sustain driving method proposed in [8] reduces the peak values and rms values of the inductor currents, which then leads to the conduction loss of the inductors to be reduced. However, its circuit has two external inductors and four external capacitors, thus the proposed circuit in [8] is still bulky.

To overcome these drawbacks, a sustainer with primary-side integration of DC-DC converters and energy recovery (SPIDER) circuits for AC PDP is proposed as shown in Fig. 3. The proposed circuit integrates the DC/DC power stage and driving stage into one circuit. Not only the proposed circuit can supply the energy to the PDP driver, but also it recovers the energy stored in the PDP, which means it has very desirable advantages such as a simpler structure, less mass, fewer power devices, and lower cost. Moreover, the ZVS of primary side switches ($R$, $F$) and secondary side switches can always be guaranteed by the magnetizing and energy recovery currents, respectively.

II. PROPOSED CIRCUIT

Generally, PDPs are driven by the address display-period separation (ADS) method. Fig. 4 shows the conventional key driving waveforms of the PDP with the ADS driving method [4], [11], [12]. A 1TV-field is the time it takes to display one image, typically 16.7 msec, i.e., 60 Hz in NTSC (National Television System Committee) mode. It is divided into 8–11 sub-fields. A sub-field is a group of the light information and partitioned into three periods as reset, address and sustain periods. During the reset period, all of the PDP cells are erased and prepared to carry out the address-operation by forming adequate wall charges. Then, during the address period, selectviewwritedischarges to form an image are ignited by applying data and scan pulses to the addressing and scanning electrodes, respectively. Since address-discharge itself emits an insufficient visible light, AC high-voltage square-wave pulses generated by the X and Y driver are continuously...
Fig. 4. Voltage waveforms applied to X and Y electrodes in ADS method during 1TV-field (NTSC mode).

Fig. 5. Comparison of the conventional driving method and the proposed driving method.

Fig. 6. The equivalent circuit diagram during reset period.

Fig. 7. The equivalent circuit diagram during address period.

A. Reset Period

In reset period, rising and falling ramp waveforms are applied to Y electrodes to initialize the PDP as shown in Fig. 4. Fig. 6(a) shows the conductive path for the rising ramp waveform. When \( S_{CL} \) and \( SC_H \) are turned on and \( Y_s \) is operated in the linear region by the low gate-to-source voltage. Therefore, \( Y_s \) is operated as the current source and the current through \( Y_s \) is linearly increased as follows,

\[
I_{D,Y_s} = K_n(V_{GS} - V_{TN})^2
\]

where, \( K_n \) is the conduction parameter of the N-channel device and is given by \( K_n = \mu_c C_{ox}/2L \), and \( V_{GS} \) is the voltage between gate and source of the switch and \( V_{TN} \) is the threshold voltage of the N-channel MOSFET.

Therefore, the voltage \( V_{CP} \) across the panel capacitor \( C_P \) is linearly increased by \( I_{D,Y_s} \) and the rising ramp waveform is applied to Y electrodes. At this point, when two path switches \( X_e \) and \( X_a \) are turned off, the undesirable resonance between the transformer and \( C_P \) does not occur and the ramp waveform is linearly increased. Moreover, due to the fact that \( V_{G2} \) is turned on, 0V is applied to X electrodes.

Fig. 6(b) shows the conductive path for the falling ramp waveform. When \( SC_L \) is turned on and \( Y_s \) is operated in the linear region, the falling ramp waveform is applied to Y electrodes. Also, if \( X_e \) is turned on, \( V_e \) is applied to X electrodes.

Namely, while the conventional system requires the power supply circuit and ERC separately, the proposed system can supply the driving power and recover the energy stored in the PDP by using one combined power conversion circuit at the same time. To achieve these operation, the pulse frequency modulation (PFM) method during an address period and the pulse width modulation (PWM) method during sustain period are used to control the proposed circuit.
B. Address Period

In address period, as shown in Fig. 4, the selective cells are ignited to form a desired image by applying data and scan pulses to the X and Y electrodes, respectively. Fig. 7 shows the conductive path during address period. The LLC half bridge resonant converter of the proposed circuit supplies the power through the resonance among the leakage and magnetizing inductors of the transformer and series resonant capacitor $C_i$ [13]. In this period, since $Y_p$ is turned off, the resonant tank is not affected by the panel capacitor $C_p$. When $X_s$, $X_l$, and $X_p$ are turned on, the secondary side of the LLC half bridge resonant converter is operated as a voltage doubler rectifier composed of $Y_s$, $Y_o$, and $V_s$. Therefore, $V_s$ becomes almost equal to $0.5V_s$ and additional devices such as rectifier diodes are not required.

In the meantime, the output voltage $V_s$ of the proposed circuit can be tightly regulated by a PFM method which varies the switching frequency of $R$ and $F$ according to load condition. Especially, although the number of sustain pulses are small during the full black image, $V_s$ can be tightly controlled because this period accounts for more than 30 percent of one sub-field.

C. Sustain Period

Fig. 8 shows the equivalent circuit of the proposed circuit during sustain period. In this period, the proposed circuit operates as the power supply and ERC. Also it recovers the energy stored in PDP by the resonance between leakage inductor $L_k$ of the transformer and the panel capacitor $C_p$. Namely, as shown in Fig. 9(g), the proposed circuit builds up inductor energy stored in $PDP$ by the resonance between leakage and magnetizing inductors of the transformer and series resonant capacitor $C_i$. In this period, since $Y_p$ is turned off, the resonant tank is not affected by the panel capacitor $C_p$. When $X_s$, $X_l$, and $X_p$ are turned on, the secondary side of the LLC half bridge resonant converter is operated as a voltage doubler rectifier composed of $Y_s$, $Y_o$ and $V_s$. Therefore, $V_s$ becomes almost equal to $0.5V_s$ and additional devices such as rectifier diodes are not required.

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D. Mode Analysis during Sustain Period

For the convenience of the mode analysis at steady state, several assumptions are made as follows:

- All parasitic components except those specified in Fig. 9 are neglected.
- The input voltage $V_{PFC}$ and sustain voltage $V_s$ are constant.
- The voltage across the series resonant capacitor $V_{C_r}$ is constant as $V_{PFC}/2$.

Fig. 9 shows the equivalent circuit diagrams and key waveforms of the proposed circuit at each operation mode during sustain period. One switching cycle can be divided into two half cycles, $t_0$-$t_6$ and $t_6$-$t_{12}$. Furthermore, since the operations of two half cycles are symmetric, only the first half cycle is explained. Before $t_0$, the voltage $V_{CP}$ across $C_p$ is maintained at $-V_s$ with $Y_o$ and $X_s$ conducting. Therefore, the current $i_{t4}$ is linearly increased.

![Equivalent Circuit Diagram](image)
Key waveforms of the proposed circuit during sustain period.

**Mode 1** \((t_r-t_i)\): When \(V_C\) and \(X_C\) are turned off at \(t_i\), mode 1 begins and the voltage \(V_{PRI}\) is applied to the primary side of the transformer (i.e., \(V_{PRI}\)) with \(R\) conducting as shown in Fig. 9(a). Thus, the voltage \(V_{Cp}\) increases by the resonance between \(C_{eq}\) \((C_{eq} = C_{eq}||C_{Y2}||C_{Y2}||C_{X2}||C_{X2})\) and \(L_k\) with the initial condition \(i_{k2} = i_{k2}(t_i)\). Therefore, the voltage \(V_{Cp}(t)\) and the current \(i_{k2}(t)\) can be obtained as follows:

\[
V_{Cp}(t) = \frac{n}{L_k C_{eq}} (V_{PRI} + nV_S - V_{Cp}(t_i))(1 + \cos \omega t)
\]

\(2\)

\[
i_{k2}(t) = \frac{1}{AL_k} (-V_{PRI} + V_{Cp}(t_i) - nV_S) \sin \omega t - i_{k2}(t_i) \cos \omega t
\]

\(3\)

where,

\[
n = \frac{N_p}{N_s}, \quad A = \frac{n^2 C_{eq} + n^2 C_{eq} + C_{eq}}{L_k C_{eq} C_{eq}}
\]

**Mode 2** \((t_1-t_2)\): When \(R\) is turned off at \(t_i\), mode 2 begins. As shown in Fig. 9(b), the voltage across \(F\) is decreased toward 0V by the resonance between \(L_k\), \(C_{eq}\) and equivalent switch output capacitor \(2C_{Zvs}\). When the voltage across \(F\) becomes 0V, \(F\) can be turned on with ZVS as shown in Fig. 9(b). At the same time, \(V_{Cp}\) is continuously increasing by the resonance between \(C_{eq}\) and \(L_k\) like previous mode 1.

**Mode 3** \((t_2-t_3)\): When \(F\) is turned on at \(t_2\), mode 3 begins. Since \(F\) is turned on, the voltage \(V_{PRI}\) is maintained at \(-V_{Cp}\), as shown in Fig. 9(c). The voltage \(V_{Cp}\) is increased by resonance of \(C_{eq}\) and \(L_k\). This mode ends at \(t_3\) when \(V_{Cp}\) becomes equal to \(V_S\). \(V_{Cp}(t)\) and \(i_{k1}(t)\) can be expressed as follows:

\[
V_{Cp}(t) = V_S
\]

\(4\)

\[
i_{k1}(t) = \frac{1}{BL_k} (V_{Cp}(t_2) + nV_S) \sin \omega t - i_{k1}(t_2) \cos \omega t
\]

\(5\)

where,

\[
n = \frac{N_p}{N_s}, \quad A = \frac{1 + n^2 C_{eq}}{L_k C_{eq}}
\]

**Mode 4** \((t_3-t_4)\): When \(V_{Cp}\) is clamped at \(V_S\), the body-diodes of \(Y_2\) and \(X_2\) are conducted as shown in Fig. 9(d). Since the voltages across \(Y_2\) and \(X_2\) are 0V, \(Y_2\) and \(X_2\) can be turned on with ZVS and the voltage across the PDP is sustained at \(V_S\). Therefore, the gas discharge of the PDP is ignited at this point. Because \(V_{PRI}\) is maintained at \(-V_{Cp}\), the current \(i_{la}\) of leakage inductor begins to linearly decrease with the slope of \(-V_{Cp} + nV_S\)/\(L_k\).

**Mode 5** \((t_4-t_5)\): At this mode, the input power is transferred to the output side as a powering phase. Since \(Y_2\) and \(X_2\) are conducting as shown in Fig. 9(e), the voltage across \(C_P\) is...
The circuit operation of Mode 6 is built as shown in Fig. 9(f). At this mode, the current \( i_{12} \) through \( L_k \) is built-up to recover the energy stored in the PDP at next half cycle. This mode ends at \( t_6 \) when \( Y_n \) and \( X_i \) are turned off.

The circuit operation of \( t_6-t_{12} \) is similar to that of \( t_5-t_6 \). Subsequently, the operation from \( t_6 \) to \( t_{12} \) is repeated.

### III. EXPERIMENTAL RESULTS

To confirm the operation validity and features of the proposed circuit, a prototype for 42-inch PDP is implemented with following specifications.

- \( V_{PF} \) : 390V
- Display condition : Full White Pattern
- Number of turns : \( N_p: N_S=36:12 \)
- Resonant tank : \( L_{res}=160\mu H, L_k=20\mu H, C_k=12nF \)
- Switching frequency during address period : 90kHz
- Switching frequency during sustain period : 250kHz
- Rising and falling time for ERC : 700nsec
- Sustain voltage \( V_s \) : 207V
- Address voltage \( V_a \) : 55V
- \( V_x \) : 91V

As shown in Fig. 10(a), the PFM during address period and PWM during sustain period are implemented with one PWM IC TL494, where switching frequency of \( R \) and \( F \) can be varied by sourcing and sinking current of \( R_T \) terminal (pin 6). TL494 operates as push-pull mode by applying \( V_{ref} \) to CTRL terminal pin (pin 13) during address period. On the other hand, it operates as single-ended mode by applying 0V to CTRL terminal during sustain period. From the above-mentioned configurations, as shown in Fig. 10(b), each gate signal can be generated. Fig. 11(a) shows that the 1-TV field is composed of 11 sub-fields and each sub-field consists...
of the reset, address, and sustain periods. Fig. 11(b) and (c) show the key waveforms during reset and address period, respectively. As shown in this figure, the proposed circuit transfers the input power to each output side by resonance between \( L_s \) and \( C_p \), and each output voltage can be well regulated. Fig. 11(d) shows the key waveforms during sustain period. As shown in this figure, the proposed circuit can successfully recover the energy stored in the PDP without hard switching operation.

Table I, II and Fig 12 show the comparison of the conventional system and the proposed system. Also, Fig. 12 shows advantages such as a simple structure, less mass, fewer devices.

Table I shows the comparative results of the measured input power consumption. As shown in this table, the proposed PDP system has smaller power consumption than the conventional system by about 4W under the same conditions. As mentioned above, the conventional PDP system consists of two-stages as DC/DC and driving stages. On the other hand, since the proposed circuit is composed of only one power conversion stage. Therefore, the proposed PDP system features better efficiency than the conventional system.

Table II shows a comparison between conventional and the proposed circuit in terms of the number of devices. As shown in this table, since the proposed circuit can remove the large number of expensive devices such as power switches, diodes, inductors and energy recovery capacitors, it features a simpler structure, less mass and lower cost of production.

**IV. CONCLUSIONS**

A new sustainer with primary sided integration of DC-DC converters and energy recovery (SPIDER) circuits for AC PDP has been presented to overcome the drawbacks of conventional circuits. Since the removal of rectifier diodes and auxiliary X and Y ERCS of the conventional PDP system is possible, it features a much simpler structure and lower cost. Moreover, the ZVS of primary side switches (R, F) cannot be guaranteed by a large leakage inductor, but those of secondary side switches can also be ensured by energy recovery operation. Nevertheless, the proposed circuit can satisfactorily recover the energy stored in the PDP and regulate each output voltage at the same time. To control the proposed circuit, the PFM and PWM are implemented with only one control IC during address and sustain periods, respectively. To confirm the validity and superiority of the proposed circuit, a prototype for 42-inch PDP is implemented. As a result, the proposed system has smaller power consumption than the conventional system by about 4W with the less number of devices. Therefore, the proposed circuit is expected to enhance competitiveness in flat panel display market.

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