Interleaved ZVS DC/DC Converter with Balanced Input Capacitor Voltages for High-voltage Applications

Bor-Ren Lin†, Huann-Keng Chiang*, and Shang-Lun Wang†

†Department of Electrical Engineering, National Yunlin University of Science and Technology, Yunlin, Taiwan

Abstract

A new DC/DC converter with zero voltage switching is proposed for applications with high input voltage and high load current. The proposed converter has two circuit modules that share load current and power rating. Interleaved pulse-width modulation (PWM) is adopted to generate switch control signals. Thus, ripple currents are reduced at the input and output sides. For high-voltage applications, each circuit module includes two half-bridge legs that are connected in series to reduce switch voltage rating to \( V_{in}/2 \). These legs are controlled with the use of asymmetric PWM. To reduce the current rating of rectifier diodes and share load current for high-load-current applications, two center-tapped rectifiers are adopted in each circuit module.

The primary windings of two transformers are connected in series at the high voltage side to balance output inductor currents. Two series capacitors are adopted at the AC terminals of the two half-bridge legs to balance the two input capacitor voltages. The resonant behavior of the inductance and capacitance at the transition interval enable MOSFETs to be switched on under zero voltage switching. The circuit configuration, system characteristics, and design are discussed in detail. Experiments based on a laboratory prototype are conducted to verify the effectiveness of the proposed converter.

Keywords: Interleaved PWM, PWM converters, Switching mode power supplies

I. INTRODUCTION

High-voltage converters have been studied and proposed for railway electrical systems [1], ship electric power distribution systems [2], and three-level medium power converters [3]-[5]. Three-level or multilevel converters/inverters [3]-[5] with clamped diodes, capacitors, or series H-bridge circuits have been proposed to reduce the voltage rating of power devices. To achieve compact size, high power density, and high circuit efficiency in modern power products, power switches with high switching frequency and low voltage rating can be adopted in medium-power converters. Thus, three-level converters can use MOSFETs to limit the voltage stress of power switches to \( V_{in}/2 \). Compared with two-level converters, three-level converters have more circuit components and higher cost.

However, power switches are operated in hard switching mode if converters have high switching frequency. This condition reduces circuit efficiency. Therefore, three-level converters with soft switching techniques [6]-[13] were developed to reduce the switching losses. Thus, all power switches can be switched on at zero current switching (ZCS) or zero voltage switching (ZVS) within the desired load range. The leakage inductance or external inductance of the transformer and the output capacitance of power switches are resonant at the transition interval. The drain-to-source voltage of MOSFETs can be decreased to zero voltage before MOSFETs are switched on. Therefore, if MOSFETs are switched on under ZVS, circuit efficiency is improved to achieve high switching frequency.

This study presents an interleaved soft switching DC/DC converter for high-voltage and medium-power applications. This converter is characterized by low switching loss, ZVS turn-on, and low voltage rating of MOSFETs. Two circuit modules are adopted, and the interleaved PWM scheme is used to share load current and reduce the ripple currents at input and output capacitors. Thus, the size of the input and output capacitors is reduced. In each circuit module, two
input capacitors and two half-bridge converters are connected in series at the high voltage side to limit the voltage rating of MOSFETs to \( V_{br}/2 \). Therefore, power MOSFETs with 500 V voltage rating can be used in DC converters with 800 V input voltage. Two balance capacitors are connected in series between the AC sides of two half-bridge legs to balance two input split capacitor voltages automatically in each switching style. The primary windings of two transformers are connected in series to balance the secondary winding currents. Thus, power can be equally transferred to output load through two center-tapped rectifiers. Asymmetric PWM is adopted to generate the appropriate signals and regulate output voltage. MOSFETs can be switched on at ZVS within the desired load range on the basis of the resonant behavior of the MOSFET output capacitance and the transformer leakage inductance. The operation principle, circuit analysis, and design example of the proposed converter are discussed in detail. To verify the performance of the proposed converter, experiments are conducted with the use of a 1.8 kW prototype.

II. CIRCUIT CONFIGURATION

For a general single-phase AC/DC converter, the conventional half-bridge and full-bridge circuit topologies are adopted in the second stage DC/DC converter to regulate output voltage. The voltage stress of the power switches in these circuit topologies is set at DC input bus voltage \( V_{dc} \). Power MOSFETs with 600 V voltage stress are normally adopted for half-bridge and full-bridge converters and are used after single-phase power factor correction (PFC). For three-phase AC/DC converters with PFC function, 900 V voltage stress MOSFETs or 1200 V IGBTs are adopted in the second stage DC/DC converter. The two half-bridge converters shown in Fig. 1 are connected in series at the high voltage side to reduce the voltage rating of power switches to \( V_{dc}/2 \). Meanwhile, these converters are connected in parallel at the low-voltage side to reduce the current rating of passive and active components. The main drawback of this circuit topology is that the two input split capacitor voltages can be unbalanced and thus result in unbalanced output inductor currents.

The circuit configuration of the proposed converter is shown in Fig. 2. The DC bus voltage after three-phase PFC is normally within the range of 750 V to 800 V. Two input split capacitor voltages \( V_{dc1} \) and \( V_{dc2} \) can be automatically balanced by the clamped capacitors \( C_{cl1} \) and \( C_{cl2} \) of the proposed DC/DC converter. The proposed DC/DC converter has two circuit modules that share the load current. The interleaved PWM with a 90-degree phase shift is adopted to generate the appropriate switching signals and regulate output voltage. Thus, the ripple currents at the input and output capacitors can be reduced. Each circuit module in the proposed converter has two half-bridge converters in series. For circuit module 1, the first half-bridge converter includes \( C_{cl1}, S_1, S_2, L_{s1}, T_1, T_2, C_{cl1}, C_{o1}, D_1, D_2, L_{o1}, \) and \( C_o \). The second half-bridge converter includes the components \( C_{cl2}, S_3, S_4, L_{s2}, T_3, C_{cl2}, C_{o2}, D_3, D_4, L_{o2}, \) and \( C_o \). \( V_{dc} \) and \( V_o \) are the input and output DC bus voltages, respectively. \( C_o \) is the output capacitance, and \( R_o \) is the load resistance. \( C_{cl1} \) and \( C_{cl2} \) are the DC blocking capacitances. \( C_{o1} \) and \( C_{o2} \) are the output capacitances of MOSFETs \( S_1 \) and \( S_2 \), respectively. \( L_{o1} \) and \( L_{o2} \) are the resonant inductances, \( L_{m1} \) and \( L_{m2} \) are the magnetizing inductances and \( L_{m1}+L_{m2} \) are the output inductances of transformers \( T_1 \) and \( T_2 \), respectively. \( D_1 \) and \( D_2 \) are the rectifier diodes. The asymmetric PWM scheme is used to control MOSFETs \( S_1 \) and \( S_2 \) have the same PWM signals, whereas \( S_3 \) and \( S_4 \) have the same PWM waveforms.

![Fig. 1 Circuit configuration of two series half-bridge converter for high-input-voltage and high-current applications.](image1)

![Fig. 2 Circuit configuration of the proposed interleaved ZVS converter.]
However, $S_1$ and $S_2$ complement each other with dead time to enable the ZVS operation. The gate signals of $S_1$–$S_3$ are phase-shifted by one-fourth of the switching period with respect to the gate signals of $S_1$–$S_3$. Therefore, the inductor currents $i_{L1}$ and $i_{L2}$ are interleaved. $C_{a1}$ and $C_{a2}$ are input capacitors that split the input voltage ($V_{C1a}=V_{C3a}=V_{dc}/2$). $C_1$ and $C_2$ are connected in series between AC terminals $a$ and $b$ to balance $V_{Ca1}$ and $V_{Ca2}$ automatically. For example, the voltage across $C_{a1}$ and $C_{a2}$ is equal to $V_{Ca1}$ if $S_1$ and $S_3$ are conducting while $S_2$ and $S_4$ are in the off-state. Meanwhile, the voltage across $C_1$ and $C_2$ is equal to $V_{Ca1}$ if $S_1$ and $S_3$ are in the off-state while $S_2$ and $S_4$ are conducting. Based on the on/off states of $S_1$–$S_4$, two split capacitor voltages $V_{Ca1}=V_{Ca2}=V_{dc}/2$ and the voltage stress of $S_1$–$S_4$ are equal to $V_{dc}/2$. In the proposed converter, the primary windings of transformers $T_1$ and $T_2$ are connected in series to balance $i_{L1}$ and $i_{L2}$ automatically. In the same manner, the output inductor currents $i_{L3}$ and $i_{L4}$ are also balanced. If power is delivered through two balanced circuit modules, then the current rating of each output inductor is equal to $I_d/4$.

### III. Operation Principle

The main PWM waveforms of circuit module 1 in the proposed converter are given in Fig. 3(a). The duty cycle of $S_1$ and $S_1$ is $\delta$, and that of $S_2$ and $S_4$ is $1-\delta$. The circuit modules are controlled by an interleaved PWM scheme. The gate signals of $S_1$–$S_4$ are phase-shifted by $T_d/4$ with respect to the gate signals of $S_1$–$S_4$, respectively. Fig. 3(b) shows the main waveforms of the proposed interleaved DC/DC converter. The following assumptions about the proposed converter are made to simplify the system analysis:

1. Transformers $T_1$–$T_4$ have the same magnetizing inductance $L_r$ and turn ratio $n$;
2. Power switches $S_1$–$S_4$ and rectifier diodes $D_1$–$D_3$ are ideal;
3. Resonant capacitances $C_{1n}=C_{3n}=C_n$;
4. DC blocking capacitances $C_{a1}=C_{a2}=C_{a}=C$;
5. Input split capacitances $C_{d1}=C_{d2}$;
6. Output inductances $L_{a1}=L_{a2}=L_{a3}=L_{a4}=L_a$; and
7. $C_o$ is sufficiently large to be considered as constant output voltage $V_o$.

Circuit modules 1 and 2 exhibit the same behavior. Thus, only circuit module 1 is discussed to simplify the circuit analysis. Based on the on/off states of $S_1$–$S_4$ and $D_1$–$D_3$, eight operating modes exist in circuit module 1 during one switching cycle. Fig. 4 shows the equivalent circuits of eight operation modes in a switching cycle. $S_1$, $S_2$, and $D_1$–$D_3$ are already conducting before time $t_0$.

**Mode 1** $[t_0 \leq t_1]$: At $t_0$, $i_{L2}=i_{L4}=0$. Given that $L_{a1}=L_{a2}>>L_r$, the magnetizing inductor voltages $v_{L1}$ and $v_{L2}$ are approximately $V_{C1a/2}$ or $(V_{dc}/2-v_{C1a})/2$. The inductor currents $i_{L1}$ and $i_{L2}$ are increasing in this mode. Power is transferred from input voltage to output load in this time interval. At $t_1$, $S_1$ and $S_4$ are both off.

**Mode 2** $[t_1 \leq t_2]$: At $t_1$, $S_1$ and $S_4$ are switched off. Given that $i_{L1}(t_1)=0$, $C_1$ and $C_3$ are charged linearly, whereas $C_2$ and $C_4$ are discharged linearly. At $t_2$, $v_{C22}$ and $v_{C32}$ are equal to $V_{C2a}$ and $v_{C3a}$, respectively.

**Mode 3** $[t_2 \leq t_3]$: At $t_2$, $v_{C2a}=v_{C1a}$ and $v_{C3a}=v_{C2a}$. The primary and secondary winding voltages of $T_1$ and $T_2$ are zero voltage, such that diodes $D_1$–$D_3$ are all conducting. In this mode, $v_{L1a}=v_{L2a}=v_{L4a}$, $i_{L1}$ and $i_{L2}$ are decreased linearly, $i_{L1}$ and $i_{L3}$ decrease, $i_{L3}$ and $i_{L4}$ increase, $C_1$ and $C_3$ are continuously charged, whereas $C_2$ and $C_4$ are discharged. If the energy stored in $L_{a1}$ is greater than that stored in $C_{a1}$, then $C_2$ and $C_4$ can be discharged to zero voltage. At $t_3$, $C_2$ and $C_4$ are also discharged to zero voltage. The time interval in modes 2 and 3 are given by

\[
\Delta t_{13} = t_3 - t_1 = \frac{2C_V}{i_{L1}(t_1)} \tag{1}
\]

The dead time $t_d$ between $S_1$ and $S_2$ must be greater than the time interval $\Delta t_{13}$ to achieve ZVS turn-on for $S_2$ and $S_4$.

**Mode 4** $[t_3 \leq t_4]$: At $t_3$, $v_{C2a}=v_{C3a}=0$. Given that $i_{L1}(t_3)=0$, the
Fig. 4. Operation modes of circuit module 1 in a switching cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.
anti-parallel diodes of $S_i$ and $S_4$ are conducting. Therefore, $S_2$ and $S_3$ can be switched on at this moment to achieve ZVS. Given that $D_1-D_4$ are still in the commutation state, the inductor voltage $v_{L_1}(t)=\left(\frac{V_1}{2}-v_{C_1}\right)$ and $i_{D_1}$ is decreasing. At $t_4$, $i_{D_1}$ and $i_{D_4}$ are decreasing to zero. The current variation of $L_1$ is $\Delta_i L_1 = I_o/(2n)$. The time interval in this mode is given by

$$\Delta t_{34} = t_4 - t_3 = \frac{L_1 I_o}{2n(V_1/2 - v_{C1})} = \frac{L_2 I_o}{2n v_{C1}} \tag{2}$$

Given that $S_2$, $S_4$, and $D_1-D_4$ are conducting, the duty loss in mode 4 is expressed as

$$\delta_{loss,4} = \frac{\Delta t_{34}}{T_s} = \frac{L_1 I_o f_s}{2n v_{C1}} \tag{3}$$

**Mode 5** [$t_5 \leq t \leq t_6$]: At $t_5$, $i_{D_1}(t)=0$. In this mode, the inductor current $i_{D_1}$ decreases. Given that the duty ratio of $S_1$ and $S_1$ is less than 0.5, the average voltages of $C_{c1}$ and $C_{c2}$ are smaller and larger than $V_o/4$, respectively. Currents $i_{D_1}$ and $i_{D_2}$ decrease with the slope of $[V_{C1}/2n-V_o]/L_1$. Power is transferred from input voltage to output load in this time interval. At time $t_5$, $S_2$ and $S_4$ are switched off.

**Mode 6** [$t_6 \leq t \leq t_7$]: At time $t_6$, power switches $S_1$ and $S_4$ are switched off. Given that $i_{D_1}(t_6)$ is negative, $C_2$ and $C_4$ are charged, whereas $C_1$ and $C_3$ are discharged. At time $t_6$, $v_{C_2}$ and $v_{C_4}$ are equal to $V_1/2$ and $V_o/2$, respectively.

**Mode 7** [$t_7 \leq t \leq t_8$]: At time $t_7$, $v_{C_2}=v_{C_1}$ and $v_{C_4}=V_o/2$. The primary and secondary winding voltages of $T_1$ and $T_2$ are equal to zero voltage, such that $D_1-D_4$ are conducting, and $v_{L_1}=v_{L_2}=V_o$, $i_{D_1}$ and $i_{D_2}$ decrease, $i_{D_3}$ and $i_{D_4}$ increase, whereas $i_{D_2}$ and $i_{D_4}$ decrease. $C_1$ and $C_3$ are continuously discharged, whereas $C_2$ and $C_4$ are charged linearly. If the energy stored in $L_1$ is greater than the energy stored in $C_1-C_4$, then $C_1$ and $C_3$ can be discharged to zero voltage. At time $t_7$, $C_1$ and $C_3$ are discharged to zero voltage. The time interval in modes 6 and 7 is given by

$$\Delta t_{57} = t_7 - t_6 = \frac{2C_v V_o}{i_{D_1}(t_6)} \tag{4}$$

The dead time $t_7$ between $S_1$ and $S_4$ must be greater than the time interval $\Delta t_{57}$ to achieve ZVS turn-on for $S_1$ and $S_4$.

**Mode 8** [$t_8 \leq t \leq t_9$]: At $t_8$, $v_{C_1}=0$. Given that $i_{D_1}(t)<0$, the anti-parallel diodes of $S_1$ and $S_4$ are conducting. $S_2$ and $S_3$ can be switched on at this moment to achieve ZVS. Given that $D_1-D_4$ are all conducting, the inductor voltage $v_{L_1}(t)=(V_o/2-v_{C1})=v_{C_2}$ and $i_{D_1}$ is increasing. At $t_9$, $i_{D_1}=I_o$. The current variation of $L_1$ is $\Delta_i L_1 = I_o/(2n)$, and the time interval in this mode is expressed as

$$\Delta t_{90} = t_9 - t_8 = \frac{L_1 I_o}{2n(V_1/2 - v_{C1})} = \frac{L_2 I_o}{2n v_{C1}} \tag{5}$$

The duty loss in mode 8 is given by

$$\delta_{loss,8} = \frac{\Delta t_{90}}{T_s} = \frac{L_1 I_o f_s}{2n v_{C2}} \tag{6}$$

The circuit operations of the proposed converter in a switching cycle are finally completed.

**IV. CIRCUIT CHARACTERISTICS**

Given that $C_{c1}-C_{c4}<<C_{r1}-C_{r4}$, the charge and discharge times of $C_{c1}-C_{c4}$ at turn-on and turn-off can be neglected. Only modes 1, 4, 5, and 8 are considered in circuit module 1 to derive the voltage conversion ratio of the proposed converter. From the volt-second balance on $(L_{c1}, L_{c2}, L_{c3})$ and $(L_{c2}, L_{c3}, L_{c4})$, the average capacitor voltages $V_{C_{c1}}-V_{C_{c4}}$ are expressed as

$$V_{C_{c1}}=V_{C_{c2}}=\frac{\delta V_{in}}{2} \text{ and } V_{C_{c2}}=V_{C_{c4}}=\left(1-\delta\right)\frac{V_{in}}{2} \tag{7}$$

where $\delta$ is the duty cycle of $S_1$, $S_3$, $S_5$, and $S_7$. We apply the volt-second balance to $L_{c1}-L_{c4}$ in steady state. The voltage conversion ratio of the proposed converter is derived from

$$\frac{V_o + V_f}{V_{in}} = -2\delta^2 + \delta(2+\delta_{loss,8} - \delta_{loss,8}) - \delta_{loss,8} = \frac{4n}{V_f} \tag{8}$$

where $V_f$ is the voltage drop on diodes $D_1-D_6$. Based on (3) and (6)-(8), the output voltage can be rewritten as

$$V_o = \frac{V_{in}}{2n}\left[\delta(1-\delta) - \frac{L_1 I_o f_s}{n V_{in}}\right] - V_f \tag{9}$$

The average output inductor currents under steady state are expressed as

$$i_{L_o}=i_{D_3}(t)+i_{L_3}(t)+i_{D_4}(t)+i_{L_4}(t) \tag{10}$$

The ripple currents on output inductors are given by

$$\Delta i_{L_1} = \Delta i_{L_2} = \Delta i_{L_3} = \Delta i_{L_4} = \frac{V_{in}}{4n L_0}(\delta(1-\delta)(1-2\delta)$$

$$+ \frac{L_1 I_o f_s (3\delta - 1)}{n V_{in}} \tag{11}$$

Given that $i_{c1,c2,c3,c4}=i_{C_{c1,c2,c3,c4}}=0$, the average magnetizing currents $i_{L_{m1}}-i_{L_{m4}}$ are approximately equal to $(1-2\delta)I_o/(4n)$. The ripple currents on inductances $L_{m1}-L_{m4}$ can be expressed as

$$\Delta i_{L_m} = \frac{Y_{c1}(\delta-\delta_{loss,8})f_s}{V_{in}} = \frac{\delta}{1-\delta} \frac{\delta(1-\delta) V_{in} - L_1 I_o}{n L_m} \tag{12}$$

The maximum and minimum magnetizing currents of $L_{m1}-L_{m4}$ are given by

$$i_{L_{m,\text{max}}} = \frac{(1-2\delta)I_o}{4n} + \frac{\delta}{1-\delta} \frac{\delta(1-\delta) V_{in} - L_1 I_o}{n L_m} \tag{13}$$

The output inductances of $L_{m1}-L_{m4}$ can be obtained as

$$L_o = \frac{\left[V_{C_{c2}}/n - V_o - V_f(\delta-\delta_{loss,8})\right] f_s}{\Delta i_{L_o}}$$

$$= \frac{(1-\delta)^2 V_{in} + L_1 I_o f_s}{2n^2(1-\delta)} \tag{14}$$

The maximum and minimum output inductor currents are expressed as

$$i_{L_{o,\text{max}}} = \frac{L_1}{4} + \frac{(1-\delta)^2 V_{in}}{4n} + \frac{L_1 I_o f_s}{2n^2(1-\delta)} \tag{15}$$
The voltage stresses of $S_1$–$S_4$ are equal to $V_{in}/2$. At time $t_1$, the inductor current $i_{L1}(t_1)$ is approximated as

$$i_{L1}(t_1) \approx \frac{i_{L1,max}}{n} = \frac{L_1}{4n} \frac{(1-2\delta)I_{in} + \delta (1-\delta)V_{in}T_s}{T_s/L_1} + \frac{I_{in}}{4L_1}$$

In the same manner, the inductor current $i_{L2}(t_2)$ at $t_2$ is approximated as

$$i_{L2}(t_2) = \frac{(1-2\delta)I_{in}}{4n} \frac{(1-\delta)V_{in}T_s - L_2I_{o}/n + I_{o}}{4L_2}$$

If the energy stored in inductor $L_1$ at $t_1$ is greater than that in capacitors $C_{r1}$–$C_{r4}$, then $C_{r1}$ and $C_{r2}$ can be discharged to zero voltage. The ZVS condition of $S_1$ and $S_3$ is expressed as

$$L_1 \geq \frac{2C_r (V_{in}/2)^2}{i_{L1}(t_1)} = \frac{C_rV_{in}^2}{2i_{L1}(t_1)}$$

The ZVS condition of $S_1$ and $S_3$ is given by

$$L_2 \geq \frac{C_rV_{in}^2}{2i_{L2}(t_2 + T_s/2)} = \frac{C_rV_{in}^2}{2i_{L2}(t_2)}$$

The ZVS condition of $S_3$ and $S_5$ is shown in (24).

$$L_2 \geq \frac{C_rV_{in}^2}{2i_{L2}(t_2 + T_s/2)} = \frac{C_rV_{in}^2}{2i_{L2}(t_2)}$$

From (21)–(24), the necessary inductances $L_1$ and $L_2$ to achieve ZVS turn-on of $S_1$–$S_5$ are derived as

$$L_1 = L_2 \geq \frac{2C_rV_{in}^2}{i_{L2}^2(t_2)} = \frac{2C_rV_{in}^2}{i_{L2}^2(t_1)}$$

V. DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

The proposed converter design is presented in this section. A laboratory prototype with 1.8 kW rated power was built to test the proposed converter. The electrical specifications of the converter are $V_{in}=750$ V to 800 V, $V_o=24$ V, $I_o=75$ A, and $f_c=100$ kHz. The maximum duty cycle of $S_1$ is assumed as 0.45 at $V_{in}=750$ V and full load. The maximum duty cycle loss in modes 4 and 8 is assumed to be 15% under a full load with a duty cycle $\delta=0.5$.

$$\delta_{loss,T} = \delta_{loss,4} + \delta_{loss,8} = \frac{4L_4I_{o,full}f_c}{nV_{in,min}} = \frac{32P_{o,full}f_c}{V_{in,min}^2} = 0.15$$

Step 1: Resonant Inductance

From (26), the resonant inductance of $L_1$ can be derived as

$$L_1 = L_2 = \frac{V_{in,min}^{\delta_{loss,T}}}{32P_{o,full}f_c} \approx 14.6 \mu H$$

In the prototype circuit, the selected inductances are $L_1 = L_2 = 14 \mu H$.

Step 2: Turns ratio of $T_1$–$T_4$

If the voltage drop $V_j$ on diodes $D_1$–$D_3$ is neglected, the turns ratio of $T_1$–$T_4$ is given by

$$\delta_{loss,T} = \delta_{loss,4} = \frac{4L_4I_{o,full}f_c}{nV_{in,min}} = \frac{32P_{o,full}f_c}{V_{in,min}^2} = 0.15$$

The TDK EER-40C magnetic cores with primary and secondary winding turns of $n_p=45$ turns and $n_i=15$ turns, respectively, are adopted for transformers $T_1$–$T_4$. The magnetizing inductance of $T_1$–$T_4$ is 350 $\mu$H.

Step 3: Power switches $S_1$–$S_5$

From (17) and (18), the $rms$ currents and voltage stresses of $S_1$–$S_5$ are given by

$$i_{S_{1,2}} = i_{S_{3,4}} = i_{S_{5,6}} = i_{S_{7,8}} = \frac{i_{S_{5,6}}}{n} = \frac{i_{S_{7,8}}}{n}$$

$$= \frac{i_{S_{5,6}}}{n} = \frac{i_{S_{7,8}}}{n}$$

$$= \frac{i_{S_{5,6}}}{n} = \frac{i_{S_{7,8}}}{n}$$

$$\approx 2A$$

$$V_{S1, stress} = \ldots = V_{S8, stress} = V_{in, min}/2 = 400 V$$

IRFP460 MOSFETs with $V_{DS}=500$ V, $I_{D,max}=20$ A, $R_{DS, on}=0.27$ $\Omega$, and $C_{in}=480$ pF at 25 V are used for $S_1$–$S_5$.

Step 4: Power diodes $D_1$–$D_8$ and capacitances

The average currents and voltage stresses of $D_1$–$D_8$ are...
expressed as
\[ I_{D1} = I_{D3} = I_{D5} = I_{D7} = \delta_{\text{max}} I_o / 4 \approx 8.4A \]  
(32)
\[ I_{D2} = I_{D4} = I_{D6} = I_{D8} = (1 - \delta_{\text{min}}) I_o / 4 \approx 10.8A \]  
(33)
\[ V_{D1,\text{stress}} = V_{D3,\text{stress}} = V_{D5,\text{stress}} = V_{D7,\text{stress}} \approx \frac{\delta_{\text{max}} V_{in,\text{min}}}{n} \approx 113V \]  
(34)
\[ V_{D2,\text{stress}} = V_{D4,\text{stress}} = V_{D6,\text{stress}} = V_{D8,\text{stress}} \approx \frac{(1 - \delta_{\text{min}}) V_{in,\text{max}}}{n} \approx 154V \]  
(35)

The KC30A30 fast recovery diodes with \( V_{RMS} = 300 \text{ V} \) and \( I_f = 30 \text{ A} \) are used as the rectifier diodes \( D_1 \sim D_8 \). The selected DC blocking capacitances and the output capacitance are \( C_d = C_d = C_a = 0.2 \mu \text{F}, C_d = C_d = 470 \mu \text{F}, \) and \( C_a = 4400 \mu \text{F} \).

**Step 5:** Output filter inductances \( L_{o1} - L_{o4} \)

The ripple current on \( L_{o1} - L_{o4} \) is set to 10% of the rated inductor current. From (10), \( L_{o1} - L_{o4} \) can be obtained from

\[ L_o = \frac{V_{Vmax} T_o [1 - \delta_{\text{min}}] (1 - 2 \delta_{\text{min}})}{0.15 I_L \times 4 \pi} \approx 16 \mu \text{H} \]  
(36)

where \( L_{o1} - L_{o4} \) are set as 16 \( \mu \text{H} \) in the prototype circuit.

**Step 6:** ZVS conditions of \( S_1 \) and \( S_2 \)

The output capacitance of IRFP460 MOSFETs is 480 \( p\text{F} \) at 25 \( \text{V} \). The equivalent output capacitance \( C_o \) at \( V_o = 800 \text{ V} \) is given by

\[ C_o \approx \frac{4}{3} C_{\text{out},25} \left( \frac{25}{V_{S1,dc}} \right) \approx 4 \times 480 \times \frac{25}{400} \approx 160 \text{pF} \]  
(37)

From (21) and (22), the minimum inductor current \( i_{L1}(t) \) and \( i_{L3}(t) \) to achieve ZVS turn-on for \( S_1 \) in \( S_3 \) is obtained from

\[ |i_{L1,\text{min}}(t)| = |i_{L3,\text{min}}(t)| \geq \sqrt{\frac{C_o V_{in,\text{max}}^2}{2L_r}} \]  
(38)

If the ripple currents on the primary and secondary sides in (19) and (20) can be neglected, the minimum load current to achieve ZVS turn-on for \( S_1 \) and \( S_3 \) are approximated in (39) and (40), respectively.

\[ I_{o,\text{min},S_1,S_3} = \frac{2n |i_{L1,\text{min}}(t)|}{\delta_{\text{min}}} \approx 25A \]  
(39)
\[ I_{o,\text{min},S_2,S_4} = \frac{2n |i_{L3,\text{min}}(t)|}{(1 - \delta_{\text{min}})} \approx 19.7A \]  
(40)

From (39) and (40), \( S_1, S_3, S_2, \) and \( S_4 \) can be switched under ZVS from 25 A load (approximately 33% load) to 75 A load (100% load). Meanwhile, \( S_2, S_3, S_4, \) and \( S_5 \) can be turned on under ZVS from 19.7 A load (approximately 26% load) to 75 A load (100% load).

Fig. 5. Photograph of the experimental setup.

![Photograph of the experimental setup](image)

Fig. 6. Measured PWM waveforms of gate voltages at full load and (a) \( V_o = 750 \text{V} \) (b) \( V_o = 800 \text{V} \).

Experiments based on a laboratory prototype, with the circuit parameters derived in the previous section, are presented in this section to verify the effectiveness of the proposed converter. A photograph of the experimental setup is shown in Fig. 5. Fig. 6 shows the measured PWM waveforms of \( S_1 \sim S_6 \) at full load under different input voltages. The PWM signals of \( S_7 \sim S_9 \) were phase-shifted by half of the switching cycle with respect to PWM signals of \( S_1 \sim S_3 \), respectively. Fig. 7 gives the measured gate voltage, drain voltage, and drain current of switches \( S_1 \) and \( S_2 \) at \( V_o = 800 \text{ V} \) and 26%, 50%, and 100% load conditions. \( S_1 \) is switched on at hard switching under 26% load and at zero
Fig. 7. Measured PWM waveforms of gate voltage, drain voltage, and drain current: (a) \( S_1 \) under 26% load, (b) \( S_2 \) under 26% load, (c) \( S_1 \) under 50% load, (d) \( S_2 \) under 50% load, (e) \( S_1 \) under 100% load, and (f) \( S_2 \) under 100% load.

Voltage switching under 50% and 100% load condition. However, \( S_2 \) is switched on under ZVS from 26% load to full load. From the test results in Fig. 7, we can expect that \( S_4, S_6 \), and \( S_8 \) are also switched on under ZVS from 26% load to full load. Fig. 8 gives the measured voltage waveforms \( V_{C_{dc1}}, V_{C_{dc2}}, \) and \( V_{C_{dc1}} + V_{C_{dc2}} \) at full load and 800 V input voltage.

Fig. 8. Measured voltage waveforms \( V_{C_{dc1}}, V_{C_{dc2}} \) and \( V_{C_{dc1}} + V_{C_{dc2}} \) at full load and 800 V input voltage.

Fig. 9. Measured waveforms of \( v_{S_{1,gs}}, v_{S_{5,gs}}, i_{L_{r1}} \) and \( i_{L_{r2}} \) at full load.

Fig. 9. Measured waveforms of \( v_{S_{1,gs}}, v_{S_{5,gs}}, i_{L_{r1}} \) and \( i_{L_{r2}} \) at full load.

Three capacitor voltages \( V_{C_{dc1}}, V_{C_{dc2}}, \) and \( V_{C_{dc1}} + V_{C_{dc2}} \) are balanced. Fig. 9 shows the measured waveforms of \( v_{S_{1,gs}}, v_{S_{5,gs}}, i_{L_{r1}} \) and \( i_{L_{r2}} \) at full load. When \( S_1 \) is conducting, \( i_{L_{r1}} \) increases. Meanwhile, \( i_{L_{r2}} \) decreases if \( S_1 \) switched off. \( i_{L_{r1}} \) and \( i_{L_{r2}} \) are phase-shifted by half of a switching cycle. Fig. 10 gives the measured waveforms of \( i_{D1}, i_{D2}, i_{D5}, i_{D6}, \) and \( i_{L_{r1}} - i_{L_{r2}} \) at full load. Fig. 11 shows the output currents \( i_{L_{r1}} + i_{L_{r2}} \) and \( i_{L_{r3}} + i_{L_{r4}} \) of the two circuit modules at full load. The output currents of the two circuit modules balance each other. Fig. 12 shows the measured circuit efficiencies at different load conditions. Based on the load current and the voltage drop on rectifier diodes, the conduction losses on rectifier diodes, MOSFETs, and power semiconductors can be estimated to be approximately 5% to 6%, 1% to 2%, and 6% to 8% of the rated power, respectively. Other power losses are related to the core and copper losses on inductors and transformers, the necessary passive snubber across the rectifier diodes, and some switching losses, such as turn-off losses on MOSFETs and switching losses on rectifier diodes. The rectifier diodes can
be replaced by synchronous rectifiers to increase circuit efficiency by approximately 2% to 4%. Low loss MOSFETs and cores can also be adopted to increase circuit efficiency.

VI. CONCLUSIONS

A new parallel DC/DC converter for applications with high input voltage and high load current is presented. The proposed converter is characterized by 1) ZVS turn-on for all switches from 33% load to 100% load, 2) \( V_{in}/2 \) voltage stress of power switches, and 3) low ripple currents at input and output sides when using the interleaved PWM scheme. Two half-bridge converters are connected in series to reduce the voltage stress of power switches at \( V_{in}/2 \). Thus, MOSFETs with 500 V voltage stress are used for 800 V input voltage applications. Two series capacitors connected at the AC terminals of two half-bridge converters are used to balance two input capacitor voltages automatically. A PWM scheme is used to generate PWM signals and regulate output voltage, such that power switches can be switched on under ZVS within the desired load range. System analysis, operation mode, circuit characteristics, and design of the proposed converter are discussed in detail. Finally, experiments with the 1.8 kW prototype are conducted to verify the effectiveness of the proposed converter.

ACKNOWLEDGMENT

This project is partly supported by the National Science Council of Taiwan under Grant NSC 102-2221-E-224 -022 -MY3.

REFERENCES


Bor-Ren Lin received his B.S.E.E. degree in Electronic Engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1988 and his M.S. and Ph.D. degrees in Electrical Engineering from the University of Missouri-Columbia, USA, in 1990 and 1993, respectively. From 1991 to 1993, he was a Research Assistant with the Power Electronic Research Center, University of Missouri. Since 1993, he has been with the Department of Electrical Engineering, National Yunlin University of Science and Technology, Douliou, Taiwan, where he is currently a Distinguished Professor. He is an Associate Editor of the Institution of Engineering and Technology Proceedings—Power Electronics and the Journal of Power Electronics. His main research interests include power-factor correction, multilevel converters, active power filters, and soft-switching converters. He has authored more than 200 published technical journal papers in the area of power electronics. Dr. Lin is an Associate Editor of the IEEE Transactions on Industrial Electronics. He was the recipient of the Research Excellence Awards in 2004, 2005, 2007, and 2011 from the Engineering College of the National Yunlin University of Science and Technology. He received the Best Paper Awards in the 2007 and 2011 IEEE Conference on Industrial Electronics and Applications, Taiwan Power Electronics 2007 Conference, the IEEE-Power Electronics and Drive Systems 2009 Conference, and the 2014 IEEE-International Conference Industrial Technology.

Huann-Keng Chiang received his M.S. and Ph.D. degrees in Electrical Engineering from the National Cheng Kung University, Taiwan, in 1987 and 1990, respectively. He is a Professor in the Department of Electrical Engineering, National Yunlin University of Science and Technology, Taiwan. His research interests include automatic control, digital control, grey theory, and motor servo control.

Shang-Lun Wang is currently working toward his M.S. in Electrical Engineering in the National Yunlin University of Science and Technology, Yunlin, Taiwan, ROC. His research interests include the design and analysis of power factor correction techniques, switching mode power supplies, and soft switching converters.