A New Reclosing and Re-breaking DC Thyristor Circuit Breaker for DC Distribution Applications

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Abstract

The DC circuit breaker is essential for supplying stable DC power with the advent of DC transmission/distribution and sensitive loads. Compared with mechanical circuit breakers, which must interrupt a very large fault current due to their slow breaking capability, a solid-state circuit breaker (SSCB) can quickly break a fault current almost within 1 [ms]. Thus, it can reduce the damage of an accident a lot more than mechanical circuit breakers. However, previous DC SSCBs cannot perform the operating duty, and are not economical because many SCR are required. Therefore, this paper proposes a new DC SSCB suitable for DC grids. It has a low semiconductor conduction loss, quick reclosing and rebreaking capabilities. As a result, it can perform the operating duties of reclosing and rebreaking. The proposed DC SSCB is designed and implemented so that it is suitable for home dc distribution at a rated power of 5 [kW] and a voltage of 380 [V]. The operating characteristics are confirmed by simulation and experimental results. In addition, this paper suggests design guidelines so that it can be applied to other DC grids. It is anticipated that the proposed DC SSCB may be utilized to design and realize many DC grid systems.

Key words: DC circuit breaker, DC SSCB, Operating duty, Solid state circuit breaker (SSCB), Thyristor circuit breaker

I. INTRODUCTION

Recently, DC transmission/distribution has become a major concern because it can increase overall system power efficiency compared to existing AC transmission/distribution. Furthermore, since a lot of loads that are sensitive to short faults or voltage sags/swells are being widely utilized with the development of the IT industry, more reliable and stable power supply technologies are required [1], [2].

However, techniques regarding the stability of DC power grids are lacking compared to existing AC power grids. In addition, there is no zero crossing of the current in DC power grids while there is zero crossing of the current in AC power grids. Thus, in DC power grids there are some difficulties in breaking over-currents and short-circuit currents. In addition, unless short-circuit current is quickly cut off, more subsequent damage can occur due to electrical fires caused by electric arcs or sparks [3].

Fig. 1 shows the maximum currents and breaking times of mechanical circuit breakers and SSCBs when short faults occur in a DC Grid. The mechanical circuit breakers are capable of breaking faults in about several tens of [ms] due to their physical structure. Thus, it is difficult for mechanical circuit breakers to prevent a lot of the damage caused by short-circuit faults because of their slow break capability [4].

In contrast, the SSCB can break faults within 1 [ms] at a much lower current level than the maximum fault current level, which reduces a lot of the damage to grid devices.

Fig. 2 shows the operation of a circuit breaker. In the normal state to transmit energy, it performs the closing operation as shown in Fig. 2-(a). If a short fault occurs, it performs the breaking operation as shown in Fig. 2-(b). However, as shown Fig. 2-(c), if the power line is held in the open state for a long time without supplying electric power after a power line is restored to normal operation, the power customers may receive a lot of consequent damages due to the electric power outage. For this reason, IEC-62271-100 prescribes the circuit breaker’s operating duty that the reclosing and rebreaking operations of a circuit breaker should be able to be performed repeatedly. Therefore, a SSCB should break the fault quickly, and perform the operating duty.

There are several types of semiconductor switching...
elements such as the IGBT, GTO, GCT and SCR used to implement a SSCB. Among them the SCR is the most suitable for use in SSCBs because it is economical and its on-state loss is relatively small [5], [6]. However, since an AC SSCB using a SCR is based on AC grid characteristics that line commutation is possible, directly applying an AC SSCB to a DC grid can cause a lot of difficulties in terms of interrupting the fault current. Therefore, it is necessary to suggest a DC SSCB that is suitable for DC power grids [7]-[11].

Fig. 3 shows a previously presented DC SSCB [10]. This SSCB supplies power through the main SCR S\textsubscript{1}, and the capacitor C is charged when turning on the SCR S\textsubscript{1} and S\textsubscript{2}. If a fault occurs, the fault current is broken through the L\textsubscript{1}-C\textsubscript{1} resonance current by turning on SCR S\textsubscript{3}. This SSCB can perform the operating duty because it can recharge the capacitor. However, since many SCRs are used for the charging and recharging loop of the capacitor and the breaking loop in this SSCB, its economic feasibility is low. In addition, a complex control is required because it has many SCRs.

To overcome such shortcomings, this paper proposes a new DC SSCB that has a low semiconductor conduction loss, and quick reclosing and rebreaking capabilities. As a result, it can perform the operating duties of reclosing and rebreaking [12].

The proposed DC SSCB is designed and implemented at a rated power of 5 [kW] and a voltage of 380 [V] that is suitable for home dc distribution. The operating characteristics are confirmed by simulation and experimental results.

II. PROPOSED DC SOLID-STATE CIRCUIT BREAKER

A. Proposed DC SSCB

Fig. 5 shows the proposed DC SSCB circuit. In the normal mode of the SSCB, the energy is supplied to the load through S\textsubscript{1}, and if a short-circuit fault occurs, the fault current is quickly broken by using the L\textsubscript{1}-C\textsubscript{1} resonance current through the resonant path of S\textsubscript{3-C-L\textsubscript{1}-S\textsubscript{1}. Since the number of the auxiliary switches is only two, one (S\textsubscript{2}) for charging the commutation capacitor C and the other (S\textsubscript{3}) for breaking the
fault current, the structure of the DC SSCB is simple and economical. Furthermore, the proposed DC SSCB can perform the reclosing and rebreaking operations according to the operation duty because the recharging operation of the commutation capacitor \( C \) is possible even when a short-circuit fault lasts on the load side.

Fig. 6 shows the circuit operation modes of the proposed DC SSCB, and Fig. 7 shows the operation waveforms corresponding to each mode. As shown in Fig. 7, the operation of the proposed DC SSCB may be divided into four operation modes. The four operation modes are the charging mode \( t_1 \sim t_2 \) to charge the commutation capacitor \( C \), the normal mode \( t_2 \sim t_4 \) to supply electric power to the load, the breaking mode \( t_4 \sim t_8 \) to break the fault current, and the recharging mode \( t_8 \sim t_9 \) to recharge the commutation capacitor.

At \( t_3 \) in Fig. 7, when a short-circuit fault occurs, the fault current \( i_{S3} \) rapidly increases. At \( t_4 \), when the fault current is three or four times higher than the full load current, the short-circuit fault is detected and the breaking mode begins. When the breaking mode is completed, the recharging mode to recharge the commutation capacitor begins in order to perform reclosing of the DC SSCB.

The operating characteristics at each mode are as follows.

### B. Operation Modes

(a) Mode 1 (Charging mode: \( t_1 \sim t_1' \sim t_2 \))

Charging the capacitor \( C \) must be preceded because the proposed DC SSCB breaks the fault current by using the \( L_2 \)-\( C \) resonance current. Thus, at mode 1, the capacitor is charged...
to a certain voltage required for breaking the fault current by turning on the SCR $S_1$ and $S_2$.

At $t_2$, the charging of the commutation capacitor is already completed, the SCR $S_2$ is naturally turned off, and the normal mode of the DC SSCB begins.

At $t_3$, the voltage of the commutation capacitor is higher than the source voltage $E$ [V]. However, the charged voltage decreases due to natural discharge because the leakage resistance of the AC capacitor used in the DC SSCB is small. Thus, the voltage of the capacitor $V_C$ decreases to the source voltage $E$ [V].

(b) Mode 2 (Normal mode: $t_2$ to $t_3$)

Since mode 2 is the normal operating mode of the DC SSCB, electric energy is supplied to the load through SCR $S_1$. In addition, the DC SSCB monitors faults such as voltage sag/swell and short circuit current.

(c) Mode 3 (Normal mode: $t_3$ to $t_4$)

Mode 3 is the section where the fault current increases after a short circuit fault occurs on the load side. Although the short circuit current increases from $t_3$, the SSCB operates in the normal mode because the magnitude of the fault current is still smaller than a preset reference value to determine the presence of a short circuit fault.

(d) Mode 4 (Breaking mode: $t_4$ to $t_5$)

Mode 4 is the section where the SCR $S_1$ is turned off. At $t_4$, when the SCR $S_1$ is turned on, the $L_1$-C resonance current $i_{S3}$ begins to flow. Thus, the $L_1$-C resonance current $i_{S3}$ gradually increases. When the $L_1$-C resonance current $i_{S3}$ becomes equal to the short circuit current $i_S$ at $t_5$, $S_1$ is naturally turned off because the current $i_{S3}$ becomes 0 [A].

(e) Mode 5 (Breaking mode: $t_5$ to $t_6$)

At $t_5$, the $L_1$-C resonant current $i_{S3}$ becomes larger than the short circuit current $i_S$. Thus, at $t_5$ to $t_6$, the current $i_{D1}$ flows as much as the difference between the $L_1$-C resonance current $i_{S3}$ and the short circuit current $i_S$.

At $t_6$, the $L_1$-C resonant current $i_{S3}$ is the same as the short circuit current $i_S$, and the diode $D_1$ is turned off.

(f) Mode 6 (Breaking mode: $t_6$ to $t_7$)

At mode 6, since the SCR $S_1$ and the diode $D_1$ are turned off, the current $i_{S3}$ is the same as the short circuit current $i_S$. Therefore, the L-C resonant current flows depending on the combined inductance of the inductors $L_2$ and $L_1$.

When the L-C resonance current $i_{S3}$ gradually decreases to zero, the SCR $S_3$ is naturally turned off at $t_7$, and the capacitor C is reversely charged to the maximum voltage.

(g) Mode 7 (Breaking mode: $t_7$ to $t_8$)

Mode 7 is the section where no current flows in the DC SSCB because all of the short-circuit current flowing through each device is interrupted.

(h) Mode 8 (Recharging mode: $t_8$ to $t_9$)

Mode 8 is the section where the commutation capacitor is recharged before being discharged again in the next breaking mode. In the DC SSCB, the commutation capacitor should be recharged to a certain voltage required for the re-break before performing the next reclosing operation. If SCR $S_2$ is turned on, the capacitor is recharged through the path $S_2$-$L_2$-$D_2$-$L_1$-$C$ as shown in Fig. 6-(h). Thus, the proposed SSCB can recharge the commutation capacitors even under a short circuit fault on the load side.

When the recharging of the capacitor is complete, the SSCB should again perform the reclosing operation by turning on SCR $S_1$ regardless of the state of the load side in order to carry out the operation duty of the reclosing and rebreaking operations. When turning on SCR $S_1$, if the short fault is already removed, the SSCB works in (b) mode 2 of Fig. 6. However, if the short-circuit fault still lasts, as shown in (c) mode 3 of Fig. 6, the SSCB rebreaks the fault current in Mode 4–7 and performs the recharging of the capacitor in Mode 8.

III. DESIGN OF THE PROPOSED DC SSCB

In order to design the proposed DC SSCB, a characteristic derivation of the voltage and current in each mode is required. Each component of the proposed DC SSCB has the maximum current and voltage in the breaking mode and recharging mode. Therefore, the capacity of the device should be determined considering the breaking mode and recharging mode. The electrical characteristic of the circuit components are considered according to each mode as shown in Table II.

A. Characteristic Derivation in the Charging Mode

Fig. 8 shows an equivalent circuit of the charging mode, and Fig. 9 shows the waveforms of $i_{S3}$ and $i_{S2}$ in the charging mode. In section $t'_1$, if the SCR $S_2$ is turned on, the undamped current $i_{S2}$ flows through the capacitor.

If the charging current $i_{S2}$ is controlled as overdamped, quick break is impossible because the charging time becomes longer and too much time is spent until the SCR $S_2$ is turned off. Therefore, the condition of the undamped circuit is expressed as Equation (1), and the charging current $i_{S2}$ is derived as Equation (2).
The maximum current of the charging mode does not have to be considered because it is less than the short circuit fault current.

B. Characteristic Derivation in the Breaking Mode

Fig. 10 shows an equivalent circuit in the breaking mode (Mode 4~7: t4~t8) of the DC SSCB and Fig. 11 shows the current waveform of the devices in the breaking mode (t4~t8).

At t3~t6, the short-circuit current is as follows:

\[
i_S = i_{S1} = \frac{E}{L_S} (t - t_1) + i_{LOAD}
\]

In Fig. 6-(d), the voltage equation is the same as Equation (4) because the SCR S1 is turned on and the resistance of the loop is almost 0 [\(\Omega\)]. The L1-C resonant current is expressed as Equation (5).

Thus, the maximum current flowing through the proposed DC SSCB is equal to equation (6) when a short fault occurs.

\[
V_{S1} = -(V_C + V_{L1}) = 0
\]

\[
i_{S3} = \frac{E}{L_1} \sin \left( \frac{t - t_4}{t_L C} \right) \quad (t_4 \leq t \leq t_6)
\]

As Equation (6) implies, if the capacitance C becomes larger or the inductance of L1 becomes smaller, the peak value of the L1-C resonant current becomes larger. If the peak value of the L1-C resonant current becomes excessively larger, it is not economical because a large capacity of the SCR and diode are required. Therefore, the inductance L1 and the capacitance C should be properly selected considering the necessary ratings of SCR S3 and the diode.

If the inductance L1 is larger than the line inductance Ls, the SSCB cannot break the fault current. In order to break the fault current, the current iS3 should be higher than the short circuit current at t5~t6 in Fig. 11. Thus, if the inductance L1 is larger than the inductance Ls, the current increases faster than iS3. Thus, the current iS3 cannot be higher than the current iS.

The line inductance Ls varies depending on the installation environment of the SSCB and the point where the short circuit occurs. The line inductance Ls can be measured when the shortest short circuit fault point is determined. Since the line inductance Ls measured in experimental setup of this paper is 64 [\(\mu\)H], the inductance L1 should be less than about 60 [\(\mu\)H]. The inductor L1 in this paper is designed to be 25 [\(\mu\)H].

The capacitance C should be selected in order to secure the tq (turn-off time) of the SCR S1. Fig. 12 shows the circuit turn-off time tq guaranteed by the circuit topology, and the device turn-off time td of the SCR S1 provided by the datasheets.

In order for SCR S1 to be turned off completely, the applied anode-to-cathode voltage V_{S1} should maintain a negative voltage for a longer duration than the device tq. In
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other words, the circuit turn-off time $t_q$ should be longer than the device turn-off time $t_{q_d}$ of the SCR $S_1$ as expressed in equation (7).

$$t_{q_d} < t_q \quad (7)$$

Since the SCR $S_1$ and the diode $D_1$ are connected in parallel, as shown in Fig. 10, the reverse voltage of the SCR $S_1$ is equal to the on-drop voltage of the diode. Therefore, if the conduction time of the diode corresponding to the circuit $t_q$ satisfies equation (7), the SCR $S_1$ can be turned off completely.

Fig. 13 shows the circuit turn-off time $t_q$ for the main SCR $S_1$ when the line inductance $L_0$, the inductor $L_1$, and the capacitor $C$ vary. When the commutation capacitor $C$ becomes larger, the circuit turn-off time $t_q$ becomes longer. Therefore, if a sufficiently large capacitance is chosen, the SCR $S_1$ can be turned off stably. However, since too large a capacitor may be expensive, the capacitance $C$ should be selected properly large, while ensuring that the circuit $t_q$ is longer than the device $t_{q_d}$.

The device $t_{q_d}$ shown in the data sheet of the SCR $S_1$ is about 50[us] under a test condition voltage of 50[V]. In the proposed DC SSCB, since the reverse voltage of the SCR $S_1$ is kept as low as the on-drop voltage, about 1.2[V], of the diode $D_1$, the actual device $t_{q_d}$ increases to approximately 1.8 times longer than the datasheet device $t_{q_d}$. Thus, considering the actual device $t_{q_d}$ of 90(=50[us]x1.8) [us], shown in Fig. 13, the capacitance $C$ should be selected, as shown in Fig. 13, so that the circuit $t_q$ may be longer than the actual device $t_{q_d}$ of 90 [us]. In this paper, when selecting a capacitance of 100 [uF], the device $t_{q_d}$ of 110 [us] is secured.

The rated voltage of the commutation capacitor $C$ should be determined by section $t' \sim t_7$ in Fig. 12. The capacitor $C$ begins charging in the reverse direction, and has a maximum charging voltage $V_{C_{\text{max}}}$ at $t_7$. Therefore, the maximum voltage $V_{C_{\text{max}}}$ of the commutation capacitor $C$ can be obtained by equation (8)–(11).

$$V_C(t_7) = E \cdot \cos \left( \frac{t_7 - t'}{\sqrt{L_1 C}} \right) \quad (8)$$

$$i_{S_3}(t_7) = i_S(t_7) = \frac{E}{L_s} (t_7 - t_3) + i_{LOAD} \quad (9)$$

$$i_{S_3}(t) = i_{S_3}(t_7) \cdot \cos \left( \frac{t - t_7}{\sqrt{L_s + L_1}} \right) + \frac{E - V_C(t_7)}{\sqrt{L_s + L_1}} \cdot \sin \left( \frac{t - t_7}{\sqrt{(L_s + L_1) C}} \right) \quad (10)$$

$$V_{C_{\text{max}}} = -\frac{1}{C} \int_{t_7}^{t_7} i_{S_3}(t) \, dt + V_C(t_7) \quad (11)$$

Fig. 14 shows the maximum voltage $V_{C_{\text{max}}}$ of the capacitor $C$ when the inductance $L_1$ and the capacitance $C$ vary.

Fig. 15 shows the voltages of a devices that performs the breaking operation at $t \sim t_7$ of Fig. 12. As shown in Fig 15, since the SCR $S_3$ is turned on until just before $t_7$, the maximum positive voltage of the SCR $S_1$ satisfies equation (12).

$$V_{C_{\text{max}}} (t_7) = V_{S_1_{\text{max}}} (t_7) = V_{D1_{\text{max}}} (t_7) \quad (12)$$

In addition, the reverse voltage of the SCR $S_1$ is always the same as the on-drop voltage of the diode $D_1$. Therefore, the rated voltage of the SCR $S_1$ should be determined considering its forward voltage, that is, the maximum voltage of the commutation capacitor.

The current flowing through the SCR $S_1$ has a maximum value at $t_4$ in Fig. 12, and it is three or four times higher than the average current (full-load current). Since the peak non-repetitive surge current of the SCR is approximately ten times higher than the mean on-state current, the SCR $S_1$ can be selected considering only its average current.

Fig. 16 shows the maximum current of the diode $D_1$ when $L_1$ and $C$ vary. Since the maximum voltage of the diode $D_1$ is...
the same as the voltage $V_{C,\text{max}}$ of the capacitor C, the rated voltage of the diode D1 should be designed only considering the maximum voltage of the commutation capacitor C.

C. Characteristic Derivation in the Recharging Mode

Fig. 17 shows an equivalent circuit of the recharging mode. Since the SCR $S_2$ and the diode $D_2$ are turned on at $t_s$ to $t_9$, the voltage equation of the recharging mode is equal to equation (13).

The most important role of the recharging mode is to recharge the commutation capacitor to a certain voltage. It should be enough to re-break the SSCB. Therefore, the recharging current $i_{S2}$ should be under damped. The condition where the recharging current $i_{S2}$ becomes an underdamped current is equal to equation (14). The resistance R and inductor $L_2$ can be selected by equation (14).

In the recharging mode, the recharging current equation is expressed as Equation (15), and the recharging voltage equation of the commutation capacitor C is expressed as Equation (16).

$$V_{C,\text{max}} = (L_1 + L_2) \frac{d}{dt} i_{S2} + R \cdot i_{S2} + \frac{1}{C} \int_0^t i_{S2} \, dt \quad (13)$$

$$R < 2 \sqrt{\frac{L_1 + L_2}{C}} \quad (14)$$

$$i_{S2}(t) = \frac{V_{C,\text{max}}}{L \cdot \omega_d} e^{-\frac{R}{2L} \cdot \sin(\omega_d \cdot t)} \quad (15)$$

$$V_C(t_s) = \int_0^{t_s} i_{S2}(t) \, dt - V_{C,\text{max}} \quad (16)$$

Since the capacitor is charged to $E \text{ [V]}$ in the charging mode, the recharged voltage of the capacitor should be $E \text{ [V]}$ or secure $t_q$ of the SCR $S_1$. Therefore, the resistance R and the inductance $L_2$ should be selected according to equations (14)-(16) so that the recharging voltage of the commutation capacitor $V_C(t_s)$ is $E \text{ [V]}$.

All of the currents flowing through the resistance R, inductance $L_2$, SCR $S_2$, and diode $D_2$ are the same. Therefore, if the resistance R and the inductance $L_2$ are determined, the peak current of the SCR $S_2$ and the diode $D_2$ can be obtained by equation (15).

The SCR $S_2$ is turned off at $t \rightarrow t_8$ in Fig. 17. Therefore, the voltage of the SCR $S_2$ is the same as the maximum voltage $V_{C,\text{max}}$ of the commutation capacitor C.

Fig. 18 shows the equivalent circuit of the SSCB at $t_9$ of Fig. 7. At $t_9$, the recharging mode is completed. Since the SCR $S_1$ is in the off-state, the voltage $V_{S1}$ of the SCR $S_1$ is equal to $V_S$. In addition, the recharged voltage $V_C$ of the capacitor is $V_S$. Therefore, the maximum voltage $V_{S3}$ of the SCR $S_3$ is $2V_S$. 

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Fig. 14. Maximum voltage $V_{C,\text{max}}$ of capacitor when $L_1$ and C vary.

Fig. 15. Voltage of devices at $t_7$ in breaking mode.

Fig. 16. Maximum current of diode D1 when $L_1$ and C vary.

Fig. 17. Equivalent circuit of recharging mode.

Fig. 18. Equivalent circuit of SSCB at $t_9$ in Fig 7.
IV. SIMULATION AND EXPERIMENTAL RESULTS

Fig. 19 shows an experimental prototype of the proposed DC SSCB. The design specifications and system parameters of the proposed DC SSCB are shown in Table 3. The simulation results are obtained through PowerSim (PSIM version 9.1) simulation software.

A. Charging Mode

Fig. 20 shows simulation waveforms of the commutation capacitor voltage and current when the SCR $S_1$ and $S_2$ is turned on in the charging mode. Fig. 21 shows the measured waveform of Fig. 20.

B. Breaking Mode

Fig. 22 shows simulation waveforms of $i_s$, $i_{S3}$, $i_{S1}$ and $i_{D1}$ in the breaking mode, and Fig. 23 shows measured waveforms of Fig. 22. It can be seen that the SCR $S_1$ is turned off by the $L_1$-C resonant current $i_{S3}$, and that the fault current $i_s$ is broken rapidly within 300 [usec].

C. Recharging Mode

In the recharging mode of the proposed DC SSCB, it should be possible to recharge the capacitor even under a short circuit fault on the load side. Fig. 24 shows simulation waveforms of the capacitor voltage $V_c$ and the current $i_c$ in the recharging mode, and Fig. 25 shows measured waveforms.
of Fig. 24. It can be seen that the capacitor C is properly recharged by turning on the SCR S2. Therefore, Fig. 24 and 25 confirm that the proposed DC SSCB can recharge the commutation capacitor even when a short-circuit fault lasts on the load side. Thus, it is able to reclose and rebreak repeatedly in the short-circuit fault on the load side.

Fig. 26 shows the capacitor voltage Vc and the capacitor current ic when performing the operation duty of reclosing and rebreaking, and Fig. 27 shows measured waveforms. In the case of a short circuit fault that lasts it can be verified that the rebreaking operation is properly performed through the detection of the short-circuit fault as soon as the DC SSCB is reclosed.

Fig. 28 shows simulation waveforms of the current is, id1, and ic in the recharging and rebreaking modes, and Fig. 29 shows the measured waveforms of Fig. 28.

It can be seen that the DC SSCB sequentially performs breaking, recharging, reclosing, rebreaking, and recharging operations very well even when a short circuit fault lasts.

As shown in Fig. 8, 10 and 17, the stray inductance is connected to the inductor L1 or L2 in series, and it has a much lower value than the inductance L1 or L2. Therefore, they do not affect the charging, breaking and recharging operations of the SSCB. As shown in Fig. 23, the effect of the stray capacitance occurs for a short time 10 [usec] from the time when the diode D1 is turned off. However, since the resonance current caused by the stray capacitance of the diode D1 has a very low value and the SCR S1 is already in the turn-off state, it has little effect on the breaking operation of the SSCB. Therefore, there is no need to consider parasitic components such as stray inductance and stray capacitance.

V. CONCLUSIONS

Since sensitive loads and DC distribution are used widespread, the DC SSCBs are essential to maintain the high power quality of the DC grid. Therefore, this paper proposes a new DC SSCB that has low conduction loss due to its main thyristor, simple structure, and good characteristic of rapid breaking within 300 [usec] of short circuit faults. Furthermore, the manufacturing cost of the proposed DC SSCB can be reduced thanks to lower rated devices and a reduced number of auxiliary SCRs. It can also perform the operating duty of reclosing and rebreaking since the recharging operation of the capacitor is possible regardless of the fault state on the load side.

The operating characteristics of the proposed DC SSCB are verified by simulations and experiments under short circuit faults. In addition, this paper suggests design guidelines so that it can be applied to other DC grids. It is anticipated that the proposed DC SSCB may be utilized to design and realize many DC grid systems.

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REFERENCES


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