N-Type Carbon-Nanotube MOSFET Device Profile Optimization for Very Large Scale Integration

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Carbon-nanotube metal oxide semiconductor field effect transistor (CN-MOSFET) is a promising future device candidate. The electrical characteristics of 16 nm N-type CN-MOSFETs are explored in this paper. The optimum N-type CN-MOSFET device profiles with different number of tubes are identified for achieving the highest on-state to off-state current ratio ($I_{on}/I_{off}$). The influence of substrate voltage on device performance is also investigated in this paper. Tradeoffs between subthreshold leakage current and overall switch quality are evaluated with different substrate bias voltages. Technology development guidelines for achieving high-speed, low-leakage, area efficient, and manufacturable carbon nanotube integrated circuits are provided.

Keywords: Carbon nanotube array, Lower subthreshold leakage, Higher performance, Substrate bias, Charge screening effect

1. INTRODUCTION

As the complementary metal-oxide semiconductor (CMOS) technology progresses into the 22 nm regime, the fundamental limitations of silicon are felt stronger. New superior materials are needed to achieve higher performance and scalable CMOS integrated circuits in the future. Carbon-nanotube (CN) transistor is a promising candidate for replacing silicon metal oxide semiconductor field effect transistor (Si-MOSFET) [1-6]. CN transistors display desirable characteristics such as elastic carrier scattering, ballistic carrier transport, and smaller device footprint (area) as compared to conventional Si-MOSFETs [1].

Two types of CN transistors have recently attracted significant attention in the literature: Schottky Barrier (SB) controlled switch (CN-SBFET) and MOSFET-like switch (CN-MOSFET) [1-6]. CN-SBFETs are formed by directly attaching the intrinsic nanotube channels to the metal source/drain contacts. CN-SBFETs show ambipolar carrier transport. Alternatively, the CN-MOSFET displays unipolar behavior with heavily doped source and drain extension regions. CN-MOSFETs are compared in [2]. CN-MOSFETs produce higher on-state and lower leakage currents. By providing a significantly higher $I_{on}/I_{off}$ ratio, CN-MOSFETs display better scalability as compared to CN-SBFETs. CN-MOSFET is the focus of the study presented in this paper due to the superior performance as compared to the CN-SBFET.

The structure of a planar-gated N-type CN-MOSFET is shown in Fig. 1. The CNs are heavily doped with donors (n+) in the source and drain extension regions in an N-type CN-MOSFET. The nanotubes are undoped under the gate. The cross-sectional view of a CN-MOSFET is shown in Fig. 2. Multiple nanotubes are placed in parallel to form an array that produces sufficient current with a CN-MOSFET.

Inspired by the developments in CN related research, publications on novel circuit techniques for very large scale integration (VLSI) of CN-MOSFETs have recently started to appear in literature [7-11]. All of these studies are based on Stanford CN-MOSFET HSPICE compact model [12]. A multi-threshold voltage six-transistor (6-T) static random access memory (SRAM) cell using CN-MOSFETs is presented by Lin et al. in [7] to provide higher performance as compared to the 32 nm-Si-MOSFET based memory cells. The characteristics of 6-T CN-MOSFET and Si-MOSFET SRAM cells are compared by Moradinasab et al. in [8] assuming a 32 nm CMOS technology. A new CN-MOSFET SRAM cell is proposed by Ebrahimi and Afzali-Kusha in [9] to enhance the read static noise margin as compared to a conventional Si-MOSFET memory cell. A novel eight-transistor CN-MOSFET SRAM cell is proposed by Kim et al. in [10] to lower the dynamic switching power consumption.
1.44 Å. The lattice unit vector \( \mathbf{a} \) along the hexagonal lattice is \( b \geq 2.49 \) Å. The carbon to carbon inter-atomic distance along the hexagonal lattice is \( b \geq 2.49 \) Å. The lattice unit vector is characterized by \( (a_1, a_2) \). The inter-atomic distances along the lattice unit vectors are \( a = |a_1| = |a_2| = \sqrt{3} b = 2.49 \) Å. \( C_{\text{ch}} = n a_1 + m a_2 \).

Fig. 1. Three-dimensional view of a planar-gated N-type CN-MOSFET.

Fig. 2. Cross-sectional view of a multi-tube CN-MOSFET. \( W_{\text{ov}} \) is the overhang of the gate from the edge of CN array.

as compared to silicon FinFET memory circuits. A new ternary inverter is proposed by Lin et al. in [11] for lower power consumption and higher performance with the CN-MOSFET technology. The conclusions of these recent publications are however difficult to reproduce and verify. Unlike a Si-MOSFET, device size is not determined merely by the physical gate width and channel length in a CN-MOSFET. The complex relationship between device sizing and performance due to the unique material properties and nanotube array structure of a CN-MOSFET is typically overlooked in these previous publications. Device and circuit design options such as transistor sizing (number of tubes), carbon nanotube array physical structure (nanotube diameters and pitch), and choice of substrate voltage are not discussed in sufficient detail.

A thorough understanding and a careful optimization of the device structure are essential to be able to develop high-performance integrated circuits with CN transistors. A p-channel CN-MOSFET device profile optimization study for achieving high-speed carbon nanotube integrated circuits is presented in [13]. Alternatively, the electrical characteristics of 16 nm N-type CN-MOSFETs are explored from a circuit designer’s point of view in this paper. The purpose of this paper is to bridge the fledgling CN-MOSFET based novel circuit development and VLSI efforts to the underlying emerging CN technology. The optimization study is based on the Stanford CN-MOSFET HSPICE compact model [12]. The dependence of device performance on the physical geometry of carbon nanotubes is presented. The optimum high-performance device profiles that provide the maximum \( I_{\text{on}} / I_{\text{off}} \) ratio are identified. Technology development and utilization guidelines are provided to achieve high-speed, low-leakage, area efficient, and manufacturable integrated circuits with CN field effect transistors.

The paper is organized as follows. The performance-critical parameters in the physical structure of a CN-MOSFET are highlighted in Section 2. The optimization results with technology development and utilization guidelines for high-performance 16 nm N-type CN-MOSFETs are presented in Section 3. Finally, some conclusions are offered in Section 4.

2. IMPORTANT CN-MOSFET PARAMETERS

Important device parameters for modeling and performance characterization of CN-MOSFETs are highlighted in this section. The relationships among CN diameter, energy bandgap, \( I_{\text{on}} \), and \( L_{\text{ox}} \) in a CN-MOSFET are explained in Section 2.1. The distinctions among the physical gate width, physical channel width, and effective channel width in a CN-MOSFET are described in Section 2.2. The important set of physical parameters from the 16 nm CN-MOSFET technology considered in this performance optimization study is presented in Section 2.3.

2.1 Carbon-nanotube diameter

The diameter of a single-walled CN (SWCN) is specified by the chirality vector \( C_{\text{ch}} (n, m) \) as shown in Fig. 3. Both \( n \) and \( m \) are positive integers. SWCN is metallic if \( |n - m| \) is an integer multiple of 3 [14]. Alternatively, if \( |n - m| \) is not an integer multiple of 3, SWCN is a semiconductor [14]. The diameter \( (d_{\text{CN}}) \) of a single-walled CN (SWCN) with chirality vector \((n, m)\) is [14]

\[
d_{\text{CN}} = \frac{a \sqrt{n^2 + m^2} + m}{\pi}
\]

where \( a \) (2.49 Å) is the carbon to carbon inter-atomic distance along the lattice unit vectors \( a_1 \) and \( a_2 \) as shown in Fig. 3.

The energy bandgap \( (E_g) \) of carbon nanotube is inversely proportional to the nanotube diameter [14]. The diameter therefore influences both on-state and off-state currents. Appropriate choice of CN diameter is critical to achieve a high speed and energy efficient electrical switch.

2.2 Width of a CN-MOSFET

The channel is a doped piece of silicon extending between the source and drain terminals in a Si-MOSFET. The gate width is essentially the length of the (polysilicon or metal) gate that overlaps the channel area perpendicular to the direction of current flow between the source and drain in a Si-MOSFET. The definition and measurement of the gate width are however different in a CN-MOSFET. Unlike a Si-MOSFET, the channel of a CN-MOSFET is composed of an array of discrete nanotubes.
Table 1. Set of process parameters for 16 nm N-type CN-MOSFET.

<table>
<thead>
<tr>
<th>Process parameters</th>
<th>Default values for 32 nm CN-MOSFET [12]</th>
<th>Fixed values for 16 nm CN-MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>0.9 V</td>
<td>0.7 V</td>
</tr>
<tr>
<td>Physical channel length (Lp)</td>
<td>32 nm</td>
<td>16 nm</td>
</tr>
<tr>
<td>Length of doped CN source-side (Ls)</td>
<td>32 nm</td>
<td>16 nm</td>
</tr>
<tr>
<td>Length of doped CN drain-side (Ld)</td>
<td>32 nm</td>
<td>16 nm</td>
</tr>
<tr>
<td>Dielectric constant of bottom gate (Kwa)</td>
<td>SiO₂ (4)</td>
<td>SiO₂ (4)</td>
</tr>
<tr>
<td>Thick oxide</td>
<td>10 μm</td>
<td>10 μm</td>
</tr>
<tr>
<td>Top gate dielectric material (High-Kwa)</td>
<td>HfO₂ (16)</td>
<td>ZrO₂ (16)</td>
</tr>
<tr>
<td>Thickness of top gate dielectric (Twa)</td>
<td>4 nm</td>
<td>3 nm</td>
</tr>
<tr>
<td>Height of gate/source/drain contact</td>
<td>64 nm</td>
<td>60 nm</td>
</tr>
<tr>
<td>Flatband voltage of N-type CN-MOSFET (Vfbn)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Fermi level of n’ doped source/drain CN region (Efo)</td>
<td>0.6 eV (~0.8%) (uniformly distributed)</td>
<td>0.6 eV (~0.8%) (uniformly distributed)</td>
</tr>
<tr>
<td>Mean free path: intrinsic CN</td>
<td>200 nm</td>
<td>200 nm</td>
</tr>
<tr>
<td>Mean free path: doped CN</td>
<td>15 nm</td>
<td>15 nm</td>
</tr>
<tr>
<td>Interconnect capacitance</td>
<td>0.213 F/μm</td>
<td>0.3 F/μm</td>
</tr>
</tbody>
</table>

*Interconnect capacitance is estimated assuming a gate/source/drain contact height of 60 nm and a contact spacing of 16 nm.

separated by insulator as illustrated in Fig. 2. The gate width of a CN-MOSFET can be therefore defined in three different ways.

The total area of a CN-MOSFET is determined by the physical gate width (Wg) as shown in Fig. 2. Wg is determined by the inter-tube pitch, the number of tubes, the diameter of CNs, and the gate overhangs beyond the carbon nanotubes at the two ends of the channel. 

\[ W_g = s \cdot (N - 1) + d_{CN} + 2 \cdot W_{ov} \]  \[(2)\]

where \( N \) is the number of tubes in a CN-MOSFET. Inter-tube pitch (s) is the distance between the centers of two adjacent nanotubes that form the channel of a CN-MOSFET. \( W_{ov} \) is the overhang width of the gate from the edge of the CN array as shown in Fig. 2. \( W_{ov} \) helps to lower the probability of leaving uncovered carbon nanotubes in the channel area due to the mis-alignments of the gate during fabrication. In a Si-MOSFET, the overhang width of the gate from the edge of the active region is typically \( 2 \lambda \) [15]. Assuming a similar photolithographic manufacturing process for CN transistors, \( W_{ov} \) at each end is assumed to be \( 2 \lambda \) (16 nm) in this study as shown in Fig. 2.

A single CN typically provides a limited amount of current. An array of multiple nanotubes is therefore necessary to be able to produce sufficient drain-to-source current in a CN-MOSFET. The physical channel width (\( W_{ch} \)) is the total accumulated diameters of the nanotubes that form the channel in a CN-MOSFET.

\[ W_{ch} = N \cdot d_{CN} \]  \[(3)\]

The electric field lines emerging from the gate terminal penetrate into the channel area are screened by the neighboring insulated nanotubes. When a positive voltage is applied on the gate terminal of an N-type CN-MOSFET, the charge induced on the CNs interact as illustrated in Fig. 4. The gate-to-channel capacitance and the resulting current produced by a nanotube are reduced due to enhanced screening effect with decreased inter-tube spacing (pitch). Charge screening reduces the effective width of the channel, thereby degrading the device current [16, 17]. Considering the charge screening effect, the effective channel width (\( W_{eff} \)) of a CN-MOSFET is

\[ W_{eff} = N \cdot d_{CN} \cdot \alpha \]  \[(4)\]

where \( \alpha \) is the screening effect coefficient (0 < \( \alpha \) < 1). When there is only one tube per gate, \( \alpha = 1 \). For \( N > 1 \), \( \alpha \) is primarily determined by the nanotube pitch. Screening effect is also influenced by the CN diameter, the number of tubes, the supply voltage, and the channel length of the device.

The current produced by a CN-MOSFET is determined by the effective channel width \( W_{eff} \). \( W_{eff} \) depends on the intensity of the electrical interactions among the carbon nanotubes that form the channel. Alternatively, the physical gate width \( W_{g} \) depends only on the physical geometry of the device. \( W_{g} \) and \( W_{eff} \) are therefore different in a CN-MOSFET. Unlike a Si-MOSFET, \( W_{g} \) contributes only to the parasitic capacitance and physical transistor area without directly influencing the drain current pro-
duced by a CN-MOSFET.

2.3 Device scaling and parameter settings

The fixed (not considered for optimization) process parameters of the 16nm CN-MOSFETs in this study are listed in Table 1. The 'Default value for 32 nm CN-MOSFET' column includes the default device parameters of the 32 nm Stanford University CN-MOSFET technology presented in [12]. As listed in Table 1, the interconnect capacitance increases when the channel length is scaled [16]. High-performance nanotube transistors with integrated high-$k$ (~25) dielectrics (zirconium oxide thin-films) are described by Javey et al. in [18]. A high-$k$ gate oxide material ($\text{ZrO}_2$) with a dielectric constant of 25 and a nominal thickness of 3 nm is assumed here to achieve high-speed transistors.

3. OPTIMIZATION OF N-TYPE CN-MOSFET

The current produced by a CN-MOSFET depends on important physical parameters such as the diameters of nanotubes, the inter-tube pitch, and the number of tubes. These parameters determine the effective channel width and device strength. In this section, the CN diameters are optimized to maximize the $I_{on}/I_{off}$ ratio for different nanotube arrays with different effective channel widths. The influence of inter-tube pitch on device performance is evaluated with two different substrate (bottom-gate) voltages. The design tradeoffs among $I_{on}$, $I_{off}$, and $I_{on}/I_{off}$ for N-type CN-MOSFETs are presented. All of the nanotubes are assumed to be semiconducting with uniform inter-tube pitch. Imperfections such as diameter variations and metallic nanotubes during the manufacturing of CN-MOSFETs are not considered in this paper. The die temperature is assumed to be 90°C [20]. The nominal supply voltage is 0.7 V. The channel lengths of all the CN-MOSFETs considered in this paper are 16 nm ($L_g = 16$ nm).

3.1 Nanotube diameter optimization

In this section, the diameter of carbon nanotubes is optimized to achieve the maximum $I_{on}/I_{off}$ ratio. $I_{on}$ is the drain current at $V_{GS} = 0$ V and $V_{DS} = V_{DD} = 0.7$ V. $I_{off}$ is the subthreshold leakage current at $V_{GS} = 0$ V and $V_{DS} = V_{DD} = 0.7$ V.

In order to evaluate the dependence of $I_{on}$ and $I_{off}$ on the diameter of nanotubes, an N-type CN-MOSFET with 2 tubes is presented as an example next. As discussed in Section 2.2, nanotube array pitch has a strong influence on $I_{on}$ produced by a CN-MOSFET. Similarly, the maximum achievable $I_{on}/I_{off}$ is affected by the array pitch. The optimum nanotube diameter that maximizes $I_{on}/I_{off}$ is generally insensitive to the nanotube array pitch. The inter-tube pitch ($\alpha$) is assumed to be 1 μm in this section to effectively eliminate the charge screening effect (i.e., $\alpha \approx 1$) and determine the maximum $I_{on}/I_{off}$ achievable by a CN-MOSFET. The maximum performance provided by an ideal CN transistor that does not suffer from charge screening effect is identified. The range of nanotube diameters is from 0.5 nm to 3 nm. All the possible chirality vectors ($n$, $m$) that can produce the diameters in this range are considered in this study.

For a fixed number of tubes and a fixed pitch, enlarging the CN diameter enhances both $I_{on}$ and $I_{off}$ as shown in Fig. 5. The increased diameter decreases the resistance of the channel region. The source and drain resistances are also reduced due to the higher number of carriers induced in the semiconducting sub-bands as the diameter is enlarged. The variation of $I_{on}$ is particularly due to the strong modulation of the source and drain resistances with the CN diameter [21]. Subthreshold leakage current is exponentially increased with the diameter. $I_{off}$ is controlled by the energy bandgap ($E_g$) of CNs. $I_{on}$ is dominated by the band-to-band tunneling current in a CN-MOSFET [2]. The energy bandgap of CN is reduced as the diameter is increased. In the subthreshold region, particularly when a negative gate voltage is applied to an N-type CN-MOSFET, the band-to-band tunneling current is enhanced with increased diameter. The additional band-to-band leakage current ($I_{on}$) through the semiconducting sub-bands is particularly severe for high $V_{DD}$ in a CN-MOSFET [21].

When the diameter ($d_{CN}$) is increased, $I_{on}$ and $I_{off}$ are enhanced at different rates. The $I_{on}/I_{off}$ is therefore maximized at an optimum diameter ($d_{OPT} = 0.7$ nm) as shown in Figs. 5 and 6 with 0V substrate bias. Similar trends for the variation of $I_{on}$, $I_{off}$, and $I_{on}/I_{off}$ with the diameter are observed when the substrate is connected to the power supply (0.7 V) as shown in Fig. 6. The x-axis of Fig. 6 corresponds to $L_g$ when the diameter is increased from 0.5 nm to 3 nm.

The substrate can be viewed as a second (bottom) gate below a thick oxide layer in a CN-MOSFET [12]. $I_{off}$ is enhanced due to stronger channel inversion with a higher substrate voltage. The subthreshold leakage current however is also increased when the substrate voltage is higher than 0 V. An n-channel CN-MOSFET cannot be effectively cut-off provided that the substrate is connected to the power supply ($V_{DS} = V_{DD} = 0.7$ V). The maximum achievable $I_{on}/I_{off}$ and the corresponding optimum nanotube diameter are therefore reduced with a higher substrate voltage.

The variation of maximum achievable $I_{on}/I_{off}$ with the number of tubes ($1 \leq N \leq 35$) for two different substrate voltages is shown in Fig. 7. For each number of tubes, the percent enhancement of the maximum achievable $I_{on}/I_{off}$ by decreasing the substrate voltage from 0.7 V to 0 V is also shown. By connecting the substrate to the ground, the maximum $I_{on}/I_{off}$ is enhanced by up to 43% as compared to the optimum $I_{on}/I_{off}$ achievable with a higher substrate voltage.

3.2 The effect of substrate voltage on the optimum diameter

The variation of optimum nanotube diameter with the transistor size (number of tubes) for $V_{DD} = 0$ V and $V_{DD} = 0.7$ V is shown in Fig. 8. Both $d_{OPT,0}$ and $d_{OPT,0.7}$ are reduced with the increased $N$ as shown in Fig. 8. When $N$ is increased from 1 to 35, $d_{OPT,0.7}$ is reduced from 0.872 nm to 0.691 nm (a reduction of approximately 26%). Alternatively, when $V_{DD} = 0$, $d_{OPT,0}$ is reduced from
0.993 nm to 0.804 nm (a reduction of approximately 23%) with the increased transistor size (as \( N \) is increased from 1 to 35).

In addition to enhanced \( I_{\text{on}}/I_{\text{off}} \), the optimum nanotube diameter that maximizes \( I_{\text{on}}/I_{\text{off}} \) is also enlarged with a smaller substrate voltage. For \( 1 \leq N \leq 35 \), \( d_{\text{OPT,0V}} \) is 7.4% to 16.4% larger as compared to \( d_{\text{OPT,0.7V}} \) as shown in Fig. 8. A lower substrate voltage with a larger optimum diameter may be preferable for easier manufacturability. Furthermore, the increased \( d_{\text{OPT,0V}} \) has little influence on the device physical gate width (\( W_g \)) and area. \( W_g \) is typically dominated by the gate overhang width, the nanoarray pitch, and the number of nanotubes in a CN-MOSFET.

### 3.3 Device performance versus integration density tradeoffs

The ideal maximum \( I_{\text{on}}/I_{\text{off}} \) of an optimized N-type CN-MOSFET is achieved at a high inter-tube pitch (assumed to be 1 μm in Section 3.1) where the screening effect is negligible. This pitch is however impractically long from an area efficiency point of view. Shorter pitches are desirable to enhance the integration density of a chip with CN-MOSFET technology. In this section, the effect of pitch reduction on the maximum achievable \( I_{\text{on}}/I_{\text{off}} \) is evaluated.

As shown in Fig. 9 with \( N = 2 \), the optimum diameter \( d_{\text{opt}} \) is independent of the inter-tube pitch (\( s \)). The optimum diameters are maintained similar to the values illustrated in Fig. 8 when the pitch is scaled for various transistor sizes (\( 1 \leq N \leq 35 \)). As listed in Tables 2 and 3, for each \( N \), four (relatively more practical from an area efficiency point of view) pitch values (\( s \)) and the corresponding physical gate widths (\( W_g \)) are identified with two different substrate voltages. 5%, 10%, 15%, and 20% degradations from the ideal maximum \( I_{\text{on}}/I_{\text{off}} \) (that could only be achieved by an essentially ideal switch with an impractically large pitch and negligible charge screening effect) are assumed to be acceptable for implementing high performance and compact integrated circuits.

As \( N \) is increased from 1 to 35, both optimum \( I_{\text{on}}/I_{\text{off}} \) and \( W_g \) are increased. For a fixed \( N \), shorter \( s \) is desirable for a smaller device area (\( W_g \) is reduced). However, the effective channel width (\( W_e \)) is also reduced due to the enhanced charge screening effect (lower \( \alpha \)) with a shorter nanotube pitch (see Eq. (4)). The \( I_{\text{off}} \) therefore decreases with a shorter \( s \). The variation of the subthreshold leakage current with the pitch is negligible since \( I_{\text{off}} \) is primarily controlled by the \( E_g \) and \( I_{\text{btbt}} \). Lowering the pitch to reduce the device area degrades \( I_{\text{on}}/I_{\text{off}} \) as listed in Tables 2 and 3. There is therefore a tradeoff between switch performance (\( I_{\text{on}}/I_{\text{off}} \)) and area efficiency (\( W_g \)). Alternatively, as listed in Tables 2 and 3 and as discussed in Section 3.1, for the same number of tubes and similar physical gate width, the maximum achievable \( I_{\text{on}}/I_{\text{off}} \) is enhanced with \( V_{\text{sub}} = 0 \) V as compared to \( V_{\text{sub}} = 0.7 \) V. A smaller substrate voltage is therefore desirable to enhance \( I_{\text{on}}/I_{\text{off}} \) without degrading the integration density of n-channel CN-MOSFETs.

### 3.4 Uniform nanotube diameter for manufacturability with different transistor sizes

As shown in Sections 3.1 and 3.2, \( I_{\text{on}}/I_{\text{off}} \) can be maximized by manufacturing nanotubes with carefully optimized diameters \( d_{\text{opt}} \) for achieving high-speed and low-power integrated circuits. Billions of transistors with various driving strengths (various device widths) will be required to implement complex state-of-the-art integrated circuits with the carbon nanotube technology. The strength of CN-MOSFETs can be tuned by adjusting the number of tubes that form the channel as explained in Section 2. The optimum diameters are listed in Tables 2 and 3 for various sizes of N-type CN-MOSFETs with different numbers of tubes (\( 1 \leq N \leq 35 \)).

The optimum diameter for achieving the maximum \( I_{\text{on}}/I_{\text{off}} \) varies with the number of tubes (transistor size) as shown in Fig. 8.
Fabricating nanotubes with different diameters for various sizes of CN-MOSFETs on a complex chip is not practical. For low-cost and high-yield manufacturability, it is highly desirable to have only one uniform nanotube diameter (for a single-Vth CN-MOSFET technology) across a chip. The effect of a uniform diameter on the performance of various sizes of CN-MOSFETs is evaluated in this section. 35 different transistor sizes are considered (the number of tubes is varied from 1 to 35) to determine a single uniform diameter for which the Ion/Ioff degradations are smaller than those of non-uniform diameters.

Three possible uniform diameters are evaluated for various sizes of CN-MOSFETs. The average diameter (d_av) is the average value of the optimum nanotube diameters shown in Fig. 8 for 1 ≤ N ≤ 35. The maximum diameter (d_max) is the maximum d_opt determined for 1 ≤ N ≤ 35. Alternatively, the minimum diameter (d_min) is the minimum d_opt in Fig. 8 for 1 ≤ N ≤ 35. The d_max and d_min are observed for N = 1 and N = 35, respectively, since d_opt that maximizes LMAX/LMIN is reduced with increased N as illustrated in Fig. 8.

The degradation from the ideal maximum LMAX/LMIN (observed at d_opt) for d_min, d_max, and d_av when using nanotubes with a uniform diameter of d_min, d_max, and d_av, respectively, is shown in Fig. 10 when V_sub = 0 V. By using nanotubes with a uniform diameter of d_min (0.839 nm), the degradation from the ideal maximum LMAX/LMIN is maintained below 20% for 3 ≤ N ≤ 35. Further analysis for even larger transistors reveals that LMAX/LMIN degradations are maintained below the 20% demarcation line by employing a uniform diameter of 0.839 nm for 36 ≤ N ≤ 73 as well. For a single-Vth CN transistor technology where only one uniform nanotube diameter is desirable for low-cost and high-yield manufacturability, the suggested nanotube diameter is therefore 0.839 nm for n-channel CN-MOSFETs with V_sub = 0 V. For N < 3, a diameter larger than d_av is desirable for higher LMAX/LMIN. Alternatively, for N > 73, a diameter smaller than d_av is desirable to limit LMAX/LMIN degradations to less than 20%.

Similar analysis is also conducted to determine a practical uniform diameter for which the LMAX/LMIN degradations are smaller than 20% at V_sub = 0.7 V. As shown in Fig. 11, the performance degradations are maintained below 20% by using nanotubes with a uniform diameter of d_min, d_max, and d_av when using nanotubes with a uniform diameter of d_min, d_max, and d_av, respectively, is shown in Fig. 10 when V_sub = 0 V. By using nanotubes with a uniform diameter of d_min, d_max, and d_av, respectively, the degradation from the ideal maximum LMAX/LMIN is maintained below 20% for 3 ≤ N ≤ 35.

Table 2. Pitch values for 5%, 10%, 15%, and 20% degradation from the maximum achievable LMAX/LMIN with 16 nm N-type CN-MOSFETs. T = 90°C. Substrate voltage = 0.7 V.

<table>
<thead>
<tr>
<th>Number of tubes</th>
<th>Optimum diameter d_opt (nm)</th>
<th>Optimum chirality vector (n, m)</th>
<th>Maximum LMAX/LMIN (× 10^4)</th>
<th>With 5% degradation from maximum LMAX/LMIN</th>
<th>With 10% degradation from maximum LMAX/LMIN</th>
<th>With 15% degradation from maximum LMAX/LMIN</th>
<th>With 20% degradation from maximum LMAX/LMIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>N=1</td>
<td>0.993</td>
<td>(1, 12), (12, 1)</td>
<td>0.913</td>
<td>--</td>
<td>32.99</td>
<td>--</td>
<td>32.99</td>
</tr>
<tr>
<td>N=2</td>
<td>0.934</td>
<td>(3, 10), (10, 3)</td>
<td>1.530</td>
<td>10.64</td>
<td>43.57</td>
<td>7.05</td>
<td>39.98</td>
</tr>
<tr>
<td>N=6</td>
<td>0.883</td>
<td>(2, 10), (10, 2)</td>
<td>3.327</td>
<td>14.09</td>
<td>103.33</td>
<td>9.64</td>
<td>81.08</td>
</tr>
<tr>
<td>N=10</td>
<td>0.872</td>
<td>(0, 11), (11, 0)</td>
<td>4.688</td>
<td>14.65</td>
<td>164.72</td>
<td>10.05</td>
<td>123.32</td>
</tr>
<tr>
<td>N=14</td>
<td>0.839</td>
<td>(4, 8), (8, 4)</td>
<td>5.886</td>
<td>18.81</td>
<td>225.37</td>
<td>10.11</td>
<td>165.05</td>
</tr>
<tr>
<td>N=18</td>
<td>0.839</td>
<td>(4, 8), (8, 4)</td>
<td>6.949</td>
<td>14.94</td>
<td>286.82</td>
<td>10.27</td>
<td>207.43</td>
</tr>
<tr>
<td>N=22</td>
<td>0.828</td>
<td>(5, 7), (7, 5)</td>
<td>7.919</td>
<td>14.98</td>
<td>347.41</td>
<td>10.29</td>
<td>248.92</td>
</tr>
<tr>
<td>N=26</td>
<td>0.828</td>
<td>(5, 7), (7, 5)</td>
<td>8.766</td>
<td>15.04</td>
<td>408.83</td>
<td>10.34</td>
<td>291.33</td>
</tr>
<tr>
<td>N=30</td>
<td>0.804</td>
<td>(2, 9), (9, 2)</td>
<td>9.598</td>
<td>14.96</td>
<td>466.64</td>
<td>10.28</td>
<td>330.92</td>
</tr>
<tr>
<td>N=35</td>
<td>0.804</td>
<td>(2, 9), (9, 2)</td>
<td>10.600</td>
<td>15.01</td>
<td>543.14</td>
<td>10.31</td>
<td>383.34</td>
</tr>
</tbody>
</table>

*All the device sizes for 1 ≤ N ≤ 35 are considered in this optimization study. Only a small number of selected devices are listed in the table due to limited space.

Table 3. Pitch values for 5%, 10%, 15%, and 20% degradation from the maximum achievable LMAX/LMIN with 16 nm N-type CN-MOSFETs. T = 90°C. Substrate voltage = 0.7 V.

<table>
<thead>
<tr>
<th>Number of tubes</th>
<th>Optimum diameter d_opt (nm)</th>
<th>Optimum chirality vector (n, m)</th>
<th>Maximum LMAX/LMIN (× 10^4)</th>
<th>With 5% degradation from maximum LMAX/LMIN</th>
<th>With 10% degradation from maximum LMAX/LMIN</th>
<th>With 15% degradation from maximum LMAX/LMIN</th>
<th>With 20% degradation from maximum LMAX/LMIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>N=1</td>
<td>0.872</td>
<td>(0, 11), (11, 0)</td>
<td>0.789</td>
<td>--</td>
<td>32.87</td>
<td>--</td>
<td>32.87</td>
</tr>
<tr>
<td>N=2</td>
<td>0.828</td>
<td>(5, 7), (7, 5)</td>
<td>1.319</td>
<td>11.06</td>
<td>43.89</td>
<td>7.4</td>
<td>40.23</td>
</tr>
<tr>
<td>N=6</td>
<td>0.781</td>
<td>(3, 8), (8, 3)</td>
<td>2.705</td>
<td>14.7</td>
<td>106.28</td>
<td>10.17</td>
<td>83.63</td>
</tr>
<tr>
<td>N=10</td>
<td>0.781</td>
<td>(3, 8), (8, 3)</td>
<td>3.646</td>
<td>16.77</td>
<td>183.71</td>
<td>11.64</td>
<td>137.54</td>
</tr>
<tr>
<td>N=14</td>
<td>0.756</td>
<td>(1, 9), (9, 1)</td>
<td>4.388</td>
<td>16.06</td>
<td>241.54</td>
<td>11.15</td>
<td>177.71</td>
</tr>
<tr>
<td>N=18</td>
<td>0.756</td>
<td>(1, 9), (9, 1)</td>
<td>5.022</td>
<td>16.95</td>
<td>320.91</td>
<td>11.78</td>
<td>233.02</td>
</tr>
<tr>
<td>N=22</td>
<td>0.705</td>
<td>(3, 7), (7, 3)</td>
<td>5.536</td>
<td>13.14</td>
<td>308.65</td>
<td>9.10</td>
<td>223.81</td>
</tr>
<tr>
<td>N=26</td>
<td>0.705</td>
<td>(3, 7), (7, 3)</td>
<td>6.252</td>
<td>13.69</td>
<td>374.96</td>
<td>9.49</td>
<td>209.96</td>
</tr>
<tr>
<td>N=30</td>
<td>0.705</td>
<td>(3, 7), (7, 3)</td>
<td>6.906</td>
<td>14.17</td>
<td>443.64</td>
<td>9.82</td>
<td>317.49</td>
</tr>
<tr>
<td>N=35</td>
<td>0.691</td>
<td>(4, 6), (6, 4)</td>
<td>7.702</td>
<td>13.47</td>
<td>490.67</td>
<td>9.34</td>
<td>350.25</td>
</tr>
</tbody>
</table>

*All the device sizes for 1 ≤ N ≤ 35 are considered in this optimization study. Only a small number of selected devices are listed in the table due to limited space.
4. CONCLUSIONS

The influence of device physical parameters on the electrical characteristics of 16nm N-type CN-MOSFETs is explored in this paper. The optimum 16 nm device profiles are identified for different nanotube arrays at 90°C. Design guidelines are provided for the development and accurate characterization of high-speed, low-power, and compact integrated circuits with carbon-nanotube transistors.

The nanotube diameter, the inter-tube pitch, and the number of tubes per device play the most important roles in determining both the area (the physical gate width) and the performance ($I_{on}/I_{off}$) of carbon-nanotube transistors. Tradeoffs among area efficiency, $I_{on}$, and $I_{on}/I_{off}$ of N-type CN-MOSFETs are explored in this paper. Furthermore, the influence of substrate voltage on device performance is investigated. For a higher number of tubes (larger transistor size), the optimum diameter that maximizes $I_{on}/I_{off}$ is reduced. For a manufacturable, high-yield, and low-cost integrated circuit however only one uniform nanotube diameter is desirable across a chip. The degradation from the maximum achievable $I_{on}/I_{off}$ is maintained below 20% with a uniform diameter of 0.839 nm for $3 \leq N \leq 73$ when the substrate is connected to the ground. Alternatively, if the substrate is connected to the power supply, the suggested uniform nanotube diameter for high-performance and manufacturability is 0.756 nm for $3 \leq N \leq 43$.

Either increasing the diameter beyond the optimum or increasing the substrate voltage of an N-type CN-MOSFET enhances the $I_{on}$ speed enhancement is however achieved at the cost of higher leakage current and degraded $I_{on}/I_{off}$. The $I_{on}/I_{off}$ can be enhanced by increasing the pitch (weakening the charge screening effect). A larger pitch however degrades the integration density. The tradeoffs between $I_{on}/I_{off}$ and area efficiency are highlighted with this study. Practical pitch values for achieving high performance within 5%, 10%, 15%, and 20% of an ideal switch are identified.

REFERENCES

[8] M. Moradinasab, F. Karbassian, and M. Fatipour, 1st Asia Sym-


